



# SPP3052

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP3052 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as DC/DC converter and Desktop computer power management.

The package is universally preferred for commercial industrial surface mount applications

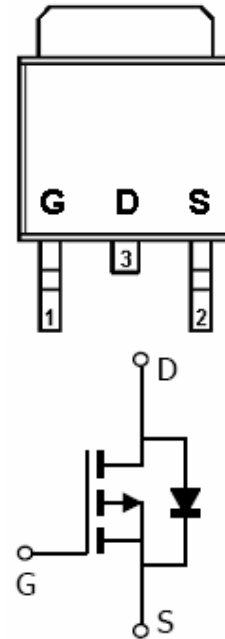
### FEATURES

- ◆ -30V/- 25A, $R_{DS(ON)}=50m\Omega@V_{GS}=-10V$
- ◆ -30V/- 16A, $R_{DS(ON)}=85m\Omega@V_{GS}=-5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L package design

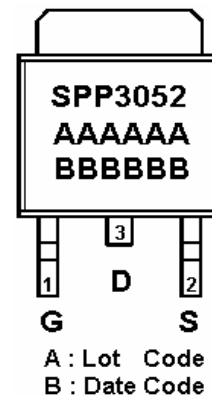
### APPLICATIONS

- Power Management in Desktop Computer
- DC/DC Converter
- LCD Display inverter

### PIN CONFIGURATION ( TO-252-2L )



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3052T252RG	TO-252-2L	SPP3052

※ Week Code : A ~ Z ( 1 ~ 26 ) ; a ~ z ( 27 ~ 52 )

※ SPP3052T252RG : Tape Reel ; Pb – Free

### ABSOLUTE MAXIMUM RATINGS

( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate –Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current( $T_J=150^{\circ}\text{C}$ )	$I_D$	$T_A=25^{\circ}\text{C}$ -25	A
		$T_A=70^{\circ}\text{C}$ -18	
Pulsed Drain Current	$I_{DM}$	-100	A
Continuous Source Current(Diode Conduction)	$I_S$	-15	A
Power Dissipation	$P_D$	$T_A=25^{\circ}\text{C}$ 40	W
		$T_A=70^{\circ}\text{C}$ 20	
Operating Junction Temperature	$T_J$	-55/150	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	105	$^{\circ}\text{C}/\text{W}$



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

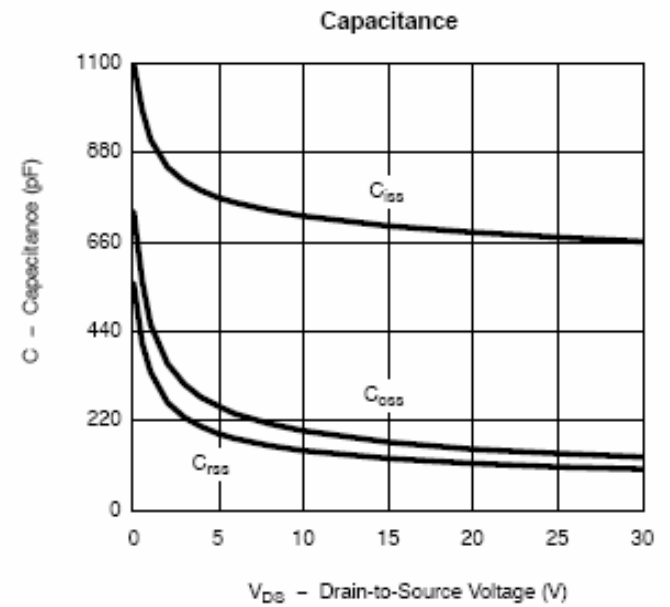
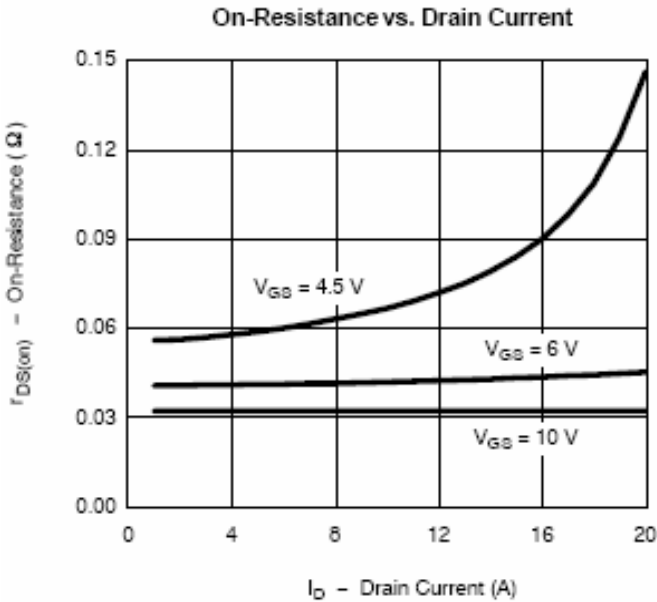
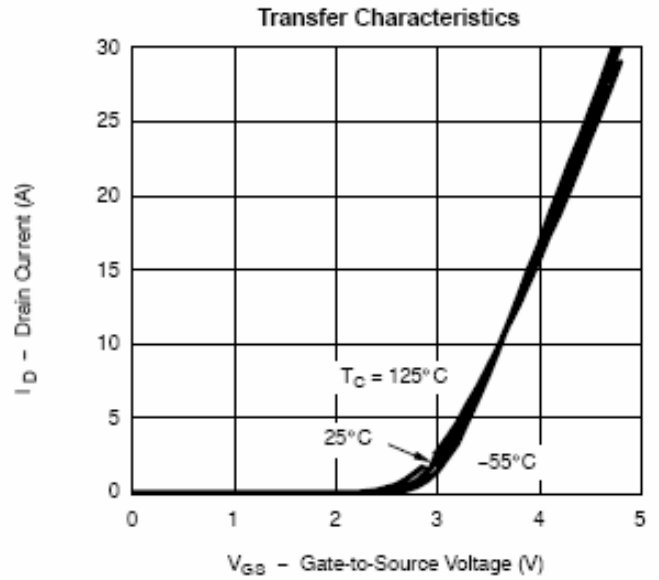
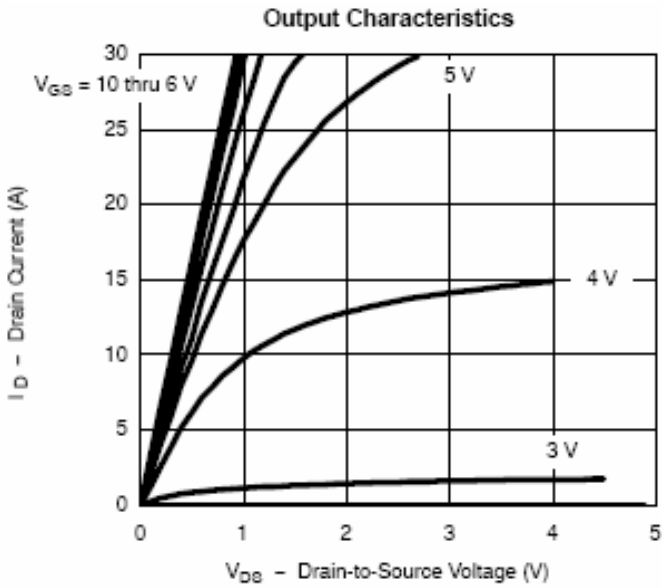
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=85^\circ C$			-5	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-25A$		0.040	0.050	$\Omega$
		$V_{GS}=-5V, I_D=-16A$		0.068	0.085	
Forward Transconductance	$g_{fs}$	$V_{DS}=-10V, I_D=-8A$		8		S
Diode Forward Voltage	$V_{SD}$	$I_S=-16A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-15V, V_{GS}=-10V$ $I_D=-3.5A$		16	24	nC
Gate-Source Charge	$Q_{gs}$			2.3		
Gate-Drain Charge	$Q_{gd}$			4.5		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		680		pF
Output Capacitance	$C_{oss}$			120		
Reverse Transfer Capacitance	$C_{rss}$			75		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-10V$ $R_G=6\Omega$		14	25	ns
	$t_r$			15	26	
Turn-Off Time	$t_{d(off)}$			42	70	
	$t_f$			30	50	



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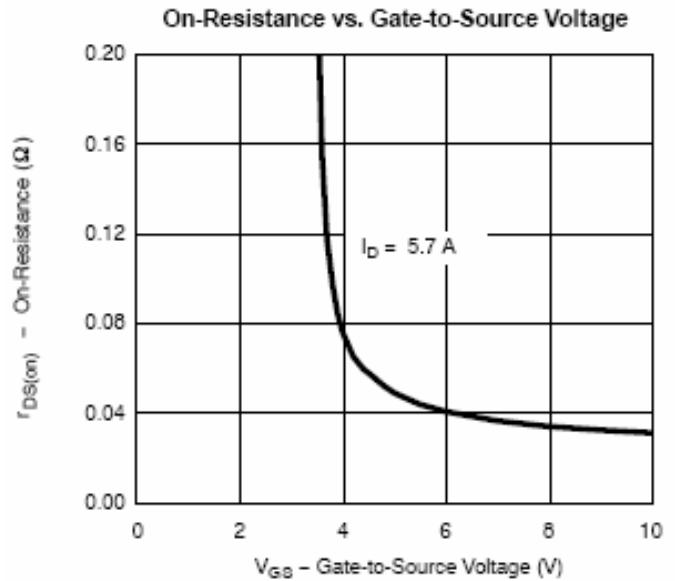
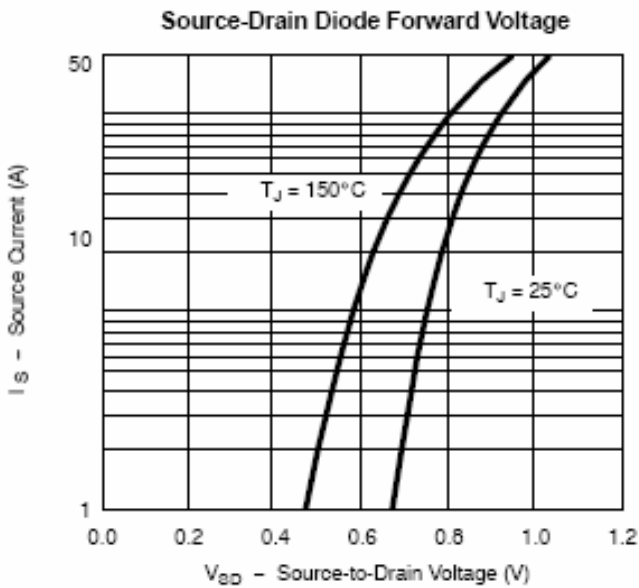
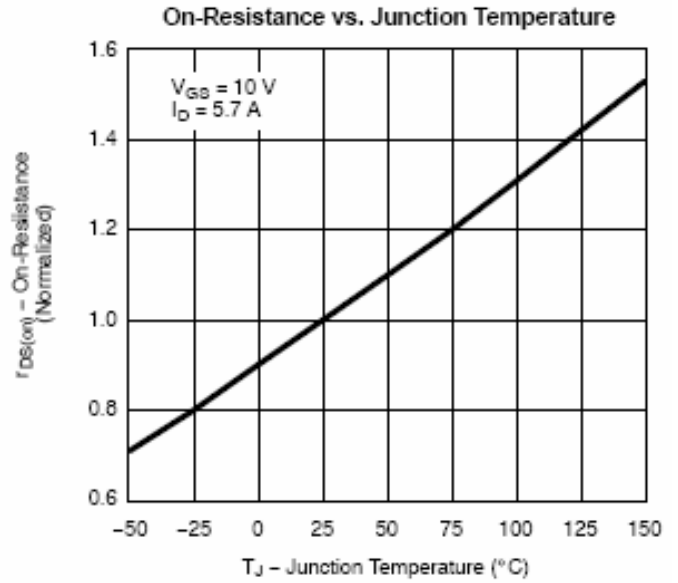
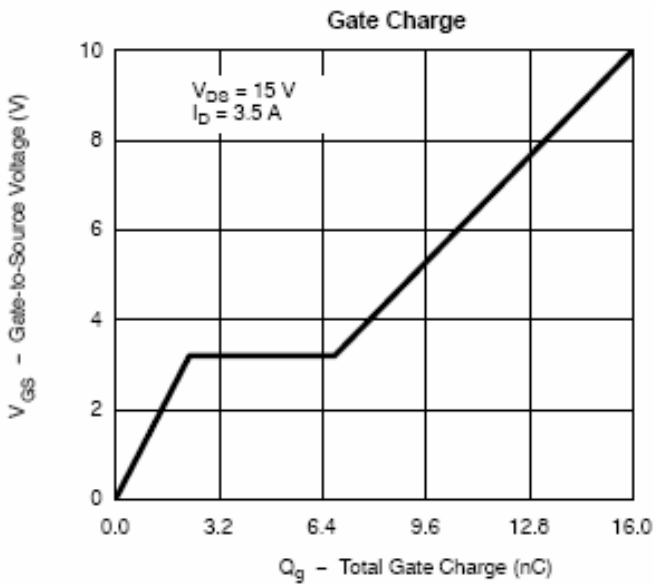
### TYPICAL CHARACTERISTICS





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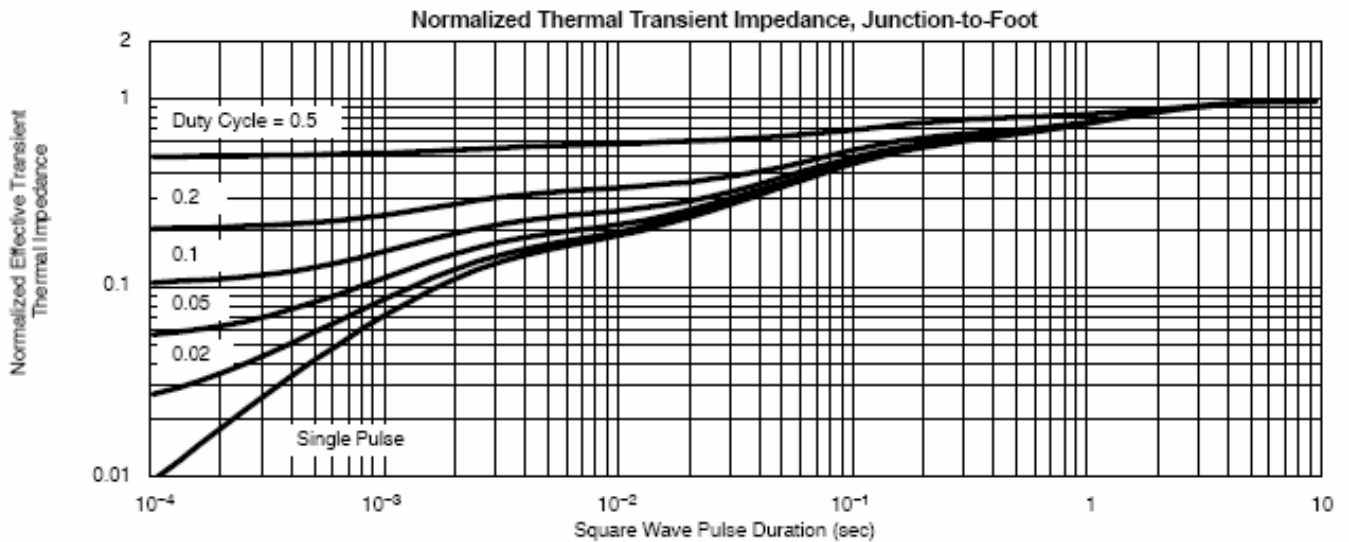
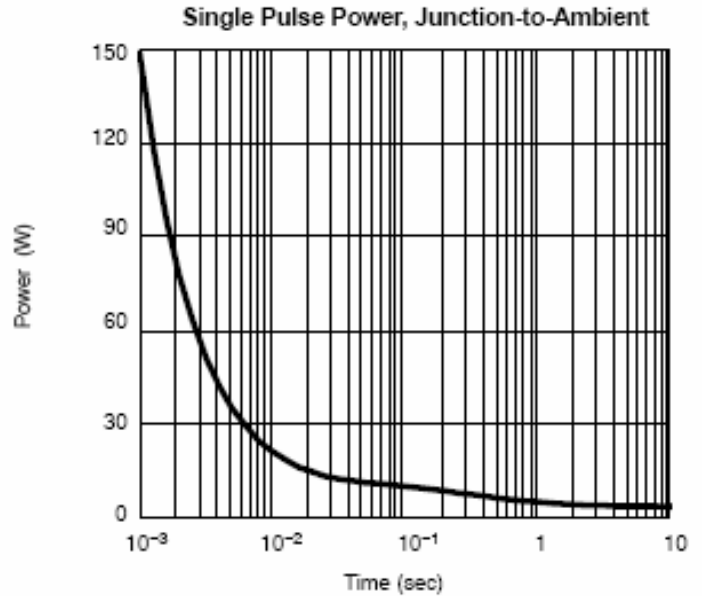
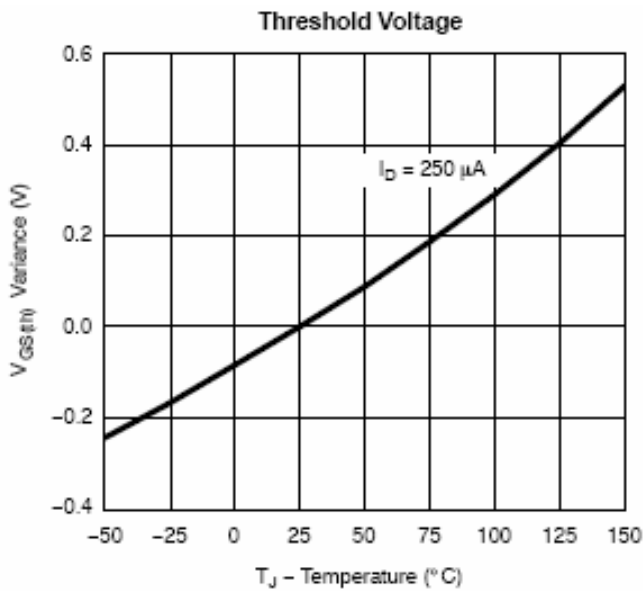
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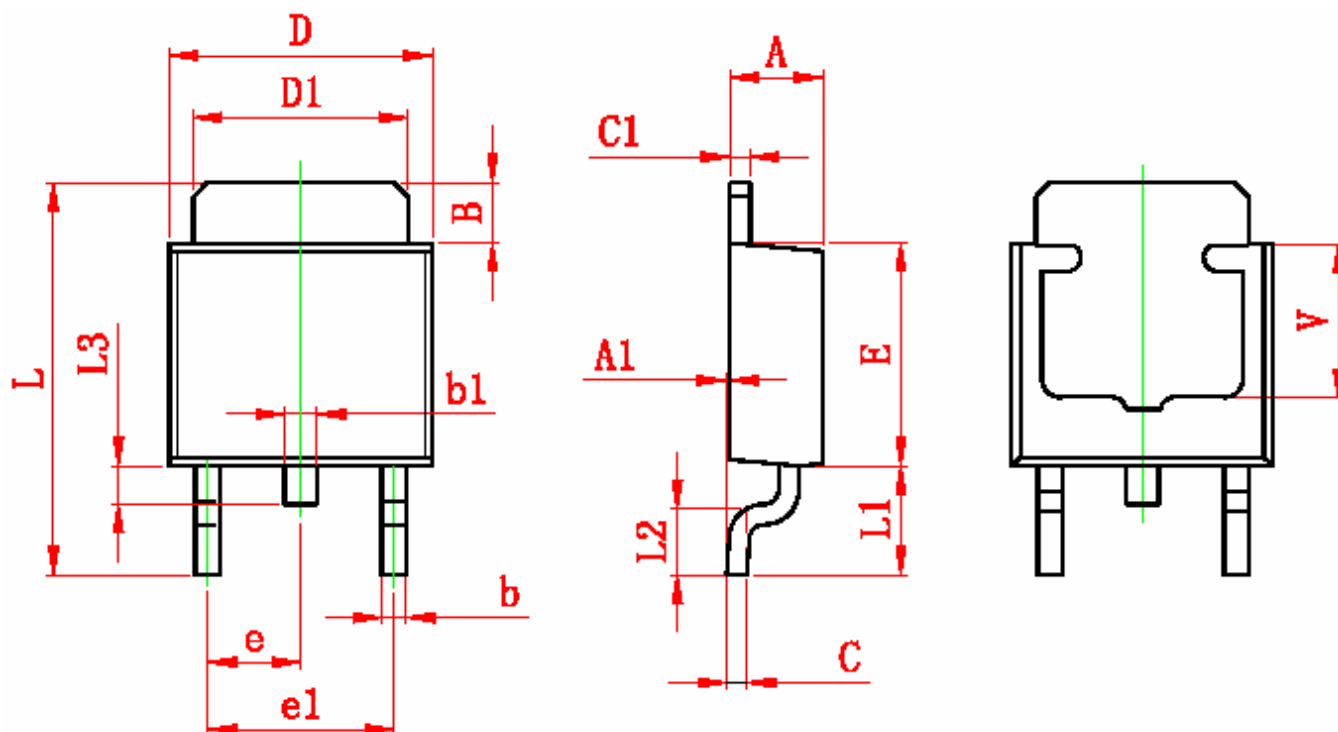




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### TO-252-2L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	



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