

### 3-CHANNEL LED DRIVER with Dimming Control

#### Features

- 3-channel individual dimming control
- Maximum output current up to 30mA per channel
- Serial-in clock frequency up to 15 MHz
- Built-in buffers for cascading clock, data, latch, and enable
- Internal power-on reset
- Schmitt trigger CMOS logic input
- Power supply voltage: 2.0V ~ 6.0V
- Output polarity selection

#### Description

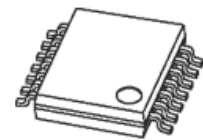
AUR6502 is a 3-channel (R, G, B) LED driver. The chip enables serial data-in and data-out interface with built-in shift registers, internal data latches and output drivers. It is designed ideally for full-color LED decorative or general lighting, signs and display applications.

Data, clock, latch, and enable output buffers can be used for cascading with next AUR6502. It is also adapted to control other MOSFETs or LED drivers especially in high power LED applications. The polarity inversion function is designed for consistent in input data and output control.

#### Applications

- LED Decorative Lighting
- LED General Lighting
- Flexible Indoor/Outdoor Video or Sign Displays

#### Package Information



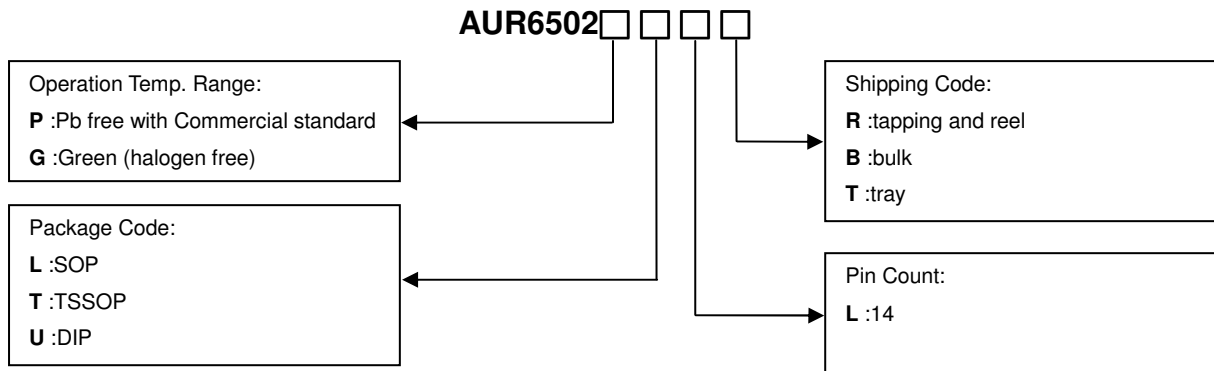
PDIP14

SOP14

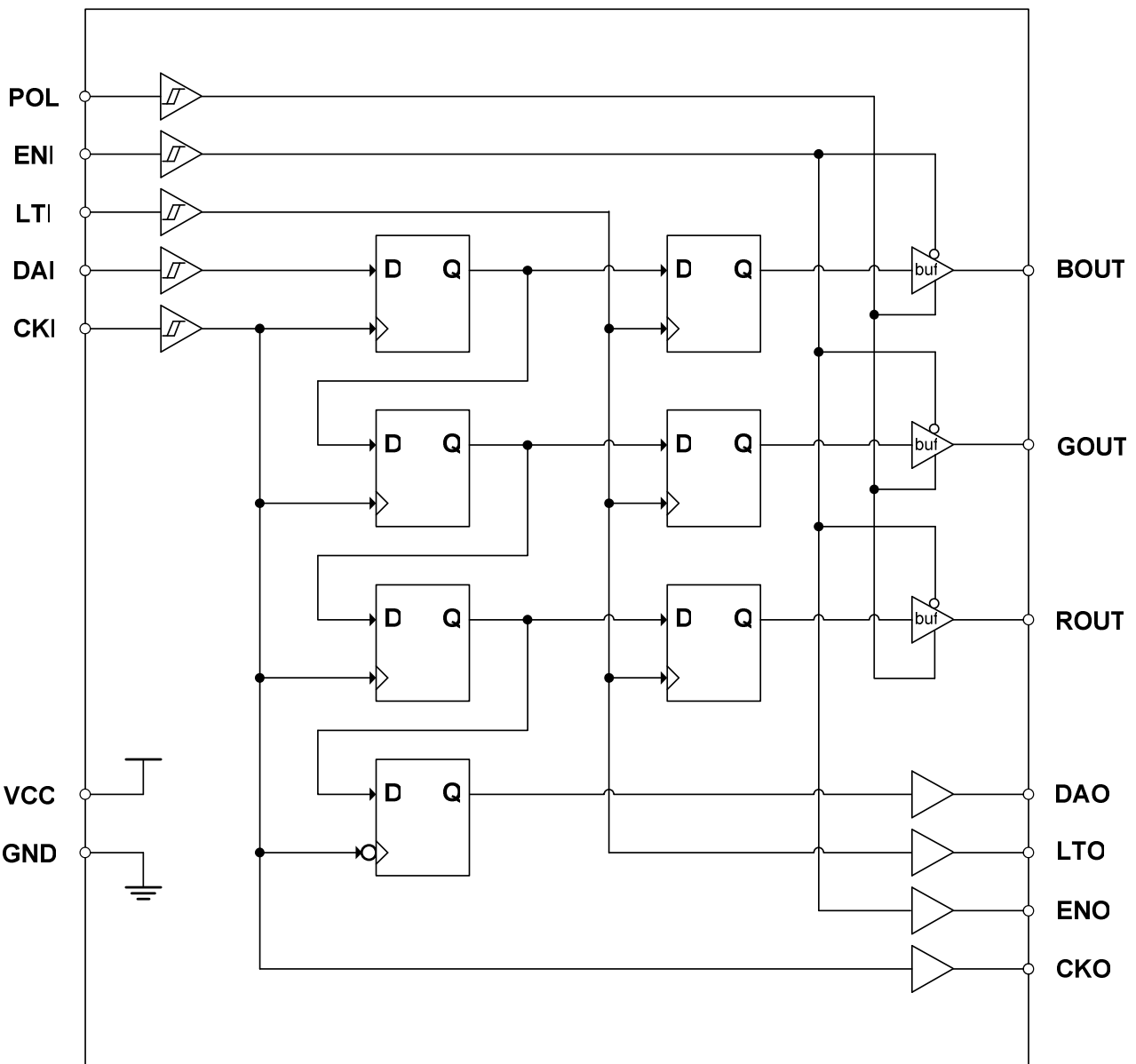
TSSOP14

COB

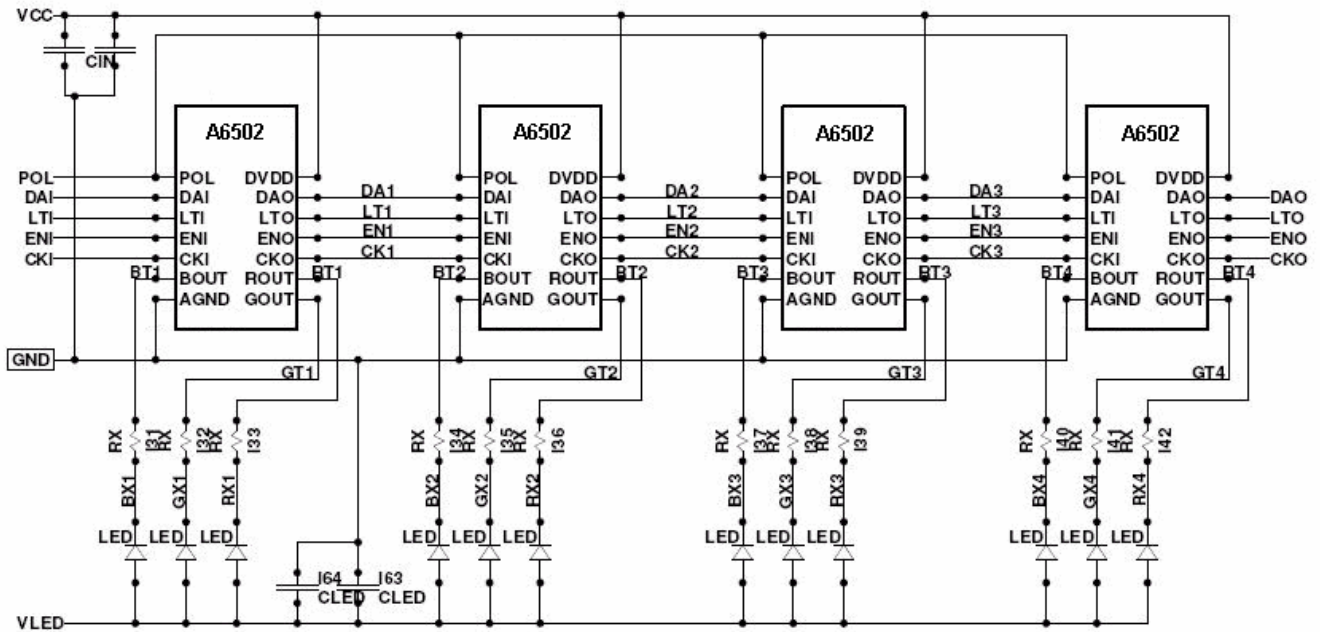
## Ordering Information



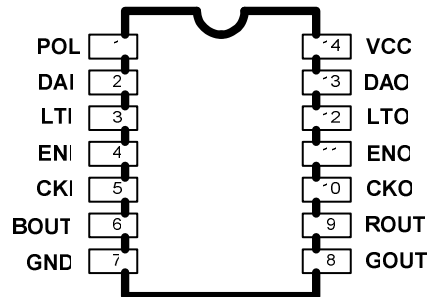
## Block Diagram



## Application Circuit

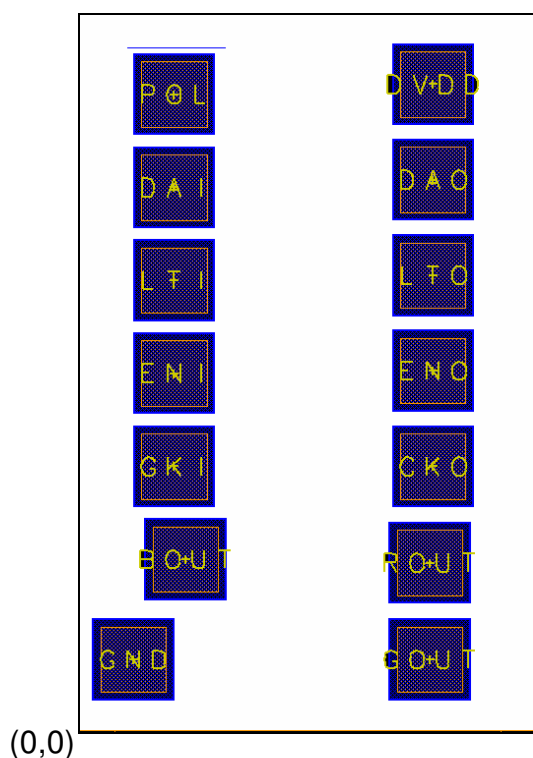


## Pin Description



PIN No.	PIN NAME	Pin Type	FUNCTION
1	POL	AI	Output polarity for data inversion: (built-in pull-down resistor) “L” for positive polarity, “H” for negative polarity.
2	DAI	DI	Serial data input
3	LTI	DI	Data-input latch pulse, latches data into internal registers at the rising edge of LTI
4	ENI	DI	Output enable control input Output is turned on when ENI = “L”, output is high impedance when ENI = “H”.
5	CKI	DI	Clock input pin for serial data transfer. Data is sampled at the rising edge of CKI
6	BOUT	AO	LED dimming control output
7	GND	GROUND	Ground Pin
8	GOUT	AO	LED dimming control output
9	ROUT	AO	LED dimming control output
10	CKO	DO	Clock output signal
11	ENO	DO	Enable output signal
12	LTO	DO	Latch output signal
13	DAO	DO	Data output signal
14	VCC	POWER	Power supply voltage input

## PAD Diagram



PAD size: 90 x 90  $\mu\text{m}^2$

Die size: 992 x 631  $\mu\text{m}^2$

PIN No.	PIN NAME	Center Coordinate	
		X	Y
1	POL	132.15	877.7
2	DAI	132.15	749.7
3	LTI	132.15	621.7
4	ENI	132.15	493.7
5	CKI	132.15	365.7
6	BOUT	147.85	237.7
7	GND	76.05	99.7
8	GOUT	483.0	99.7
9	ROUT	483.0	232.7
10	CKO	487.5	365.7
11	ENO	487.5	497.2
12	LTO	487.5	628.7
13	DAO	487.5	760.2
14	VCC	487.5	891.7

**Maximum Ratings** (  $T_a = 25^\circ\text{C}$  ,  $T_{j(\text{max})} = 140^\circ\text{C}$  )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	- 0.3 ~ 7.0	V
Logic Input Voltage	VIN	- 0.3 ~ VCC+0.3	V
Driver Output Current	IOUT	30	mA
Driver Output Voltage	VOUT	- 0.3 ~ 7.0	V
Input Clock Frequency	FCKI	15	MHz
GND Pin Current	IGND	100	mA
Power Dissipation	PD	tbd ( TSSOP14 : $T_a=25^\circ\text{C}$ ) tbd ( SOP14 : $T_a=25^\circ\text{C}$ ) tbd ( DIP14 : $T_a=25^\circ\text{C}$ )	W
Thermal Resistance	Rth(j-a)	tbd ( TSSOP14 ) tbd ( SOP14 ) tbd ( DIP14 )	$^\circ\text{C}/\text{W}$
Operating Temperature	Top	- 40 ~ 85	$^\circ\text{C}$
Storage Temperature	Tstg	- 65 ~ 150	$^\circ\text{C}$

**Recommended Operating Condition**

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC		2.0	5.0	6.0	V
Driver Output Voltage	VOUT	Driver Off			6.0	
Output Current	IOUT	(Driver) OUT (R, G, B)			30	mA
	IOH	(Logic) SERIAL-OUT			1.0	
	IOL				-1.0	
Logic Input Voltage	VIH	VCC = 3.0V ~ 5.5V	0.8VCC		VCC	V
	VIL		GND		0.2VCC	
CKI Pulse Width	twCKI	VCC = 3.0V ~ 5.5V	25			ns
Set-up Time of DAI	tsetup(D)		10			
Hold Time of DAI	thold(D)		10			
Set-up Time for LTI	tsetup(L)		20			

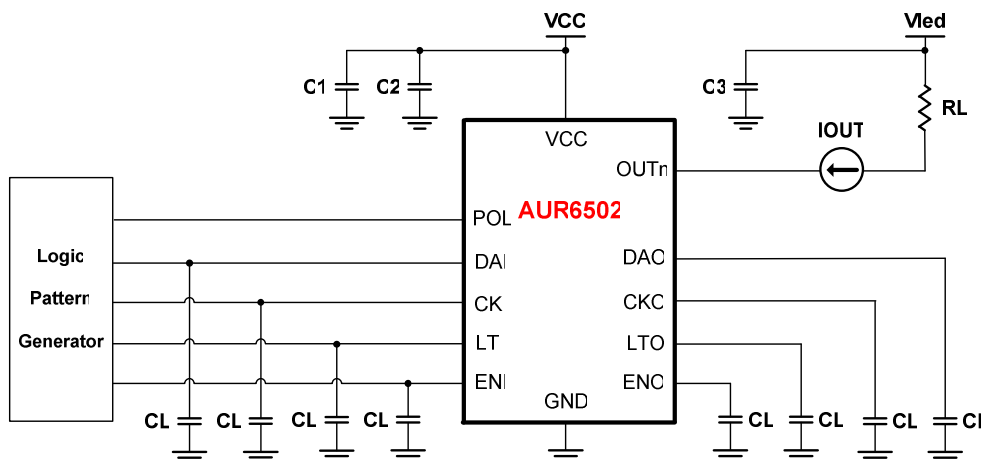
## Electrical Characteristics (VCC = 5.0V, Ta = 25°C, Tj(max) = 140°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Input Voltage 'H' Level	VIH	CMOS	0.8VCC		VCC	V
Logic Input Voltage 'L' Level	VIL	logic level	GND		0.2VCC	
Driver Output Leakage Current	IOL	VOH = 6.0V			1.0	μA
Logic Output Voltage (S-OUT)	VOL	IOL = 1mA			0.2	V
	VOH	IOH = -1mA	VCC-0.2			
Supply Current	IDD_DC	EN = VCC DC measurement		1		uA

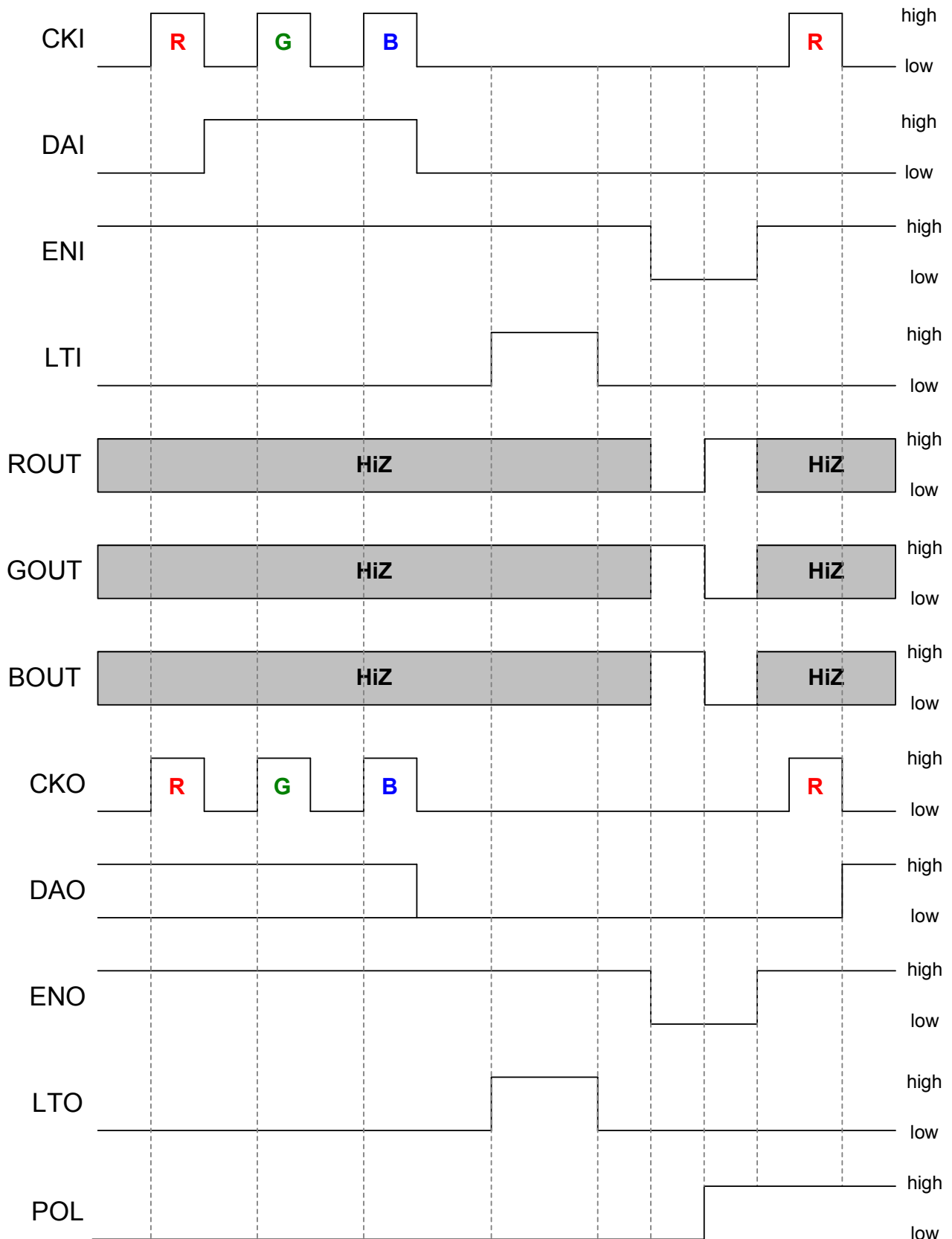
## Switching Characteristics (Ta = 25°C, Tj(max) = 140°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Propagation Delay (L→H): CKI to CKO	tpLH(C)	VCC=5.0V VIH=VCC VIL=GND RL=51Ω Vled=5.0V CL=15pF C1=1uF C2=0.1uF C3=4.7uF		10		ns	
Propagation Delay (H→L): CKI to CKO	tpHL(C)			10			
CKO to DAO	td(D)			10			
Propagation Delay (L→H): LTI to LTO	tpLH(L)			10			
Propagation Delay (H→L): LTI to LTO	tpHL(L)			10			
Propagation Delay (L→H): ENI to ENO	tpLH(E)			10			
Propagation Delay (H→L): ENI to ENO	tpHL(E)			10			
Propagation Delay (L→H): LTI to OUTn	tpLH(LO)			20			
Propagation Delay (H→L): LTI to OUTn	tpHL(LO)			20			
Propagation Delay (L→H): ENI to OUTn	tpLH(EO)			20			
Propagation Delay (H→L): ENI to OUTn	tpHL(EO)			20			
Rise Time of OUTn	tor				100		
Fall Time of OUTn	tof				100		

## Switching Test Diagram



## Timing Diagrams



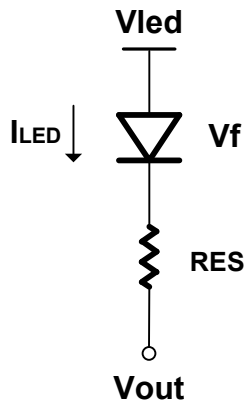


## Setting LED Current:

The output current level of individual driver is established by an external resistor RES for each channel. The value of external resistor setting LED current can be determined by the equation below. It is recommended the voltage at driver output ports should be as low as possible for consideration of power dissipation and to keep Vled stable for operating LED in constant current.

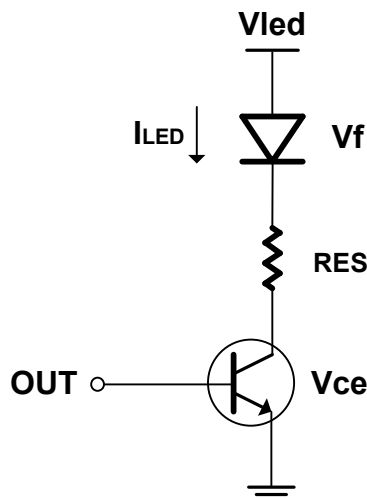
## Typical Application 1: (POL=High)

$$RES (\Omega) = [ Vled(V) - Vf(V) - Vout(V) ] / ILED(A)$$

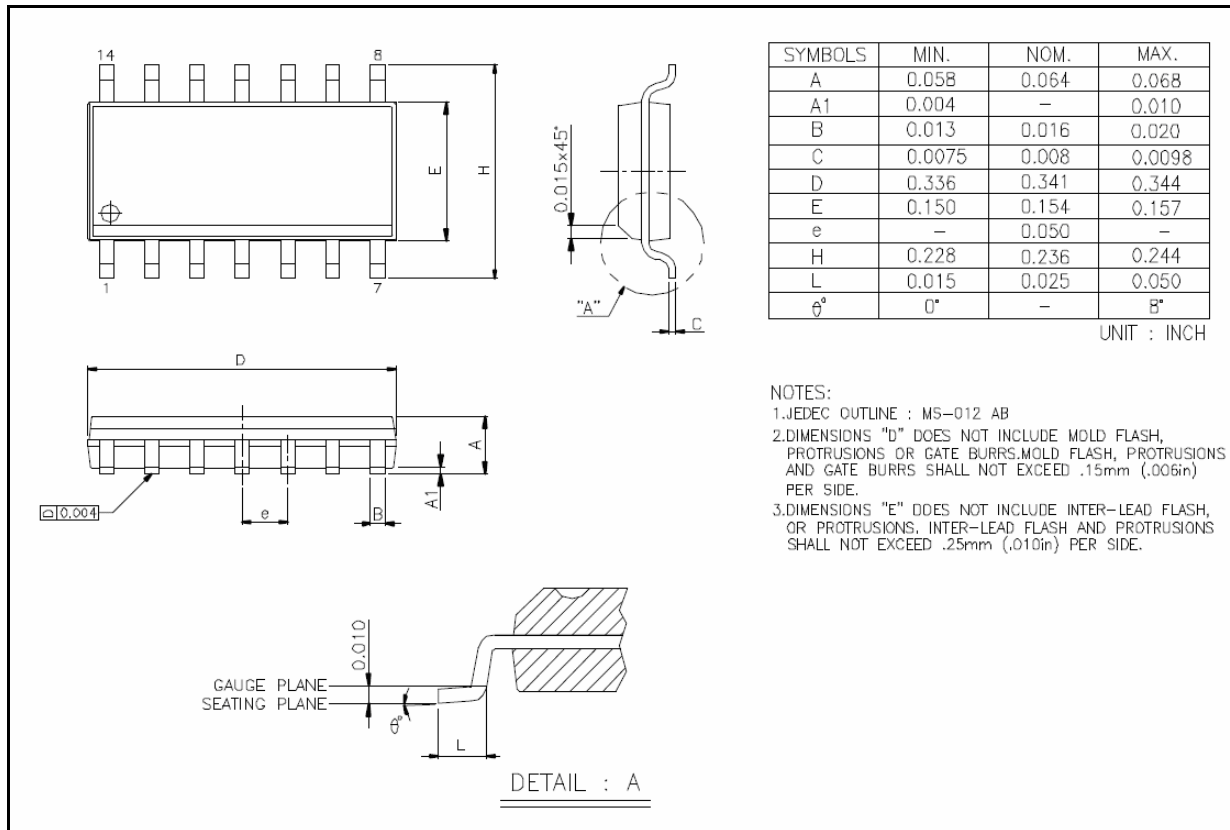


## Typical Application 2: (POL=Low)

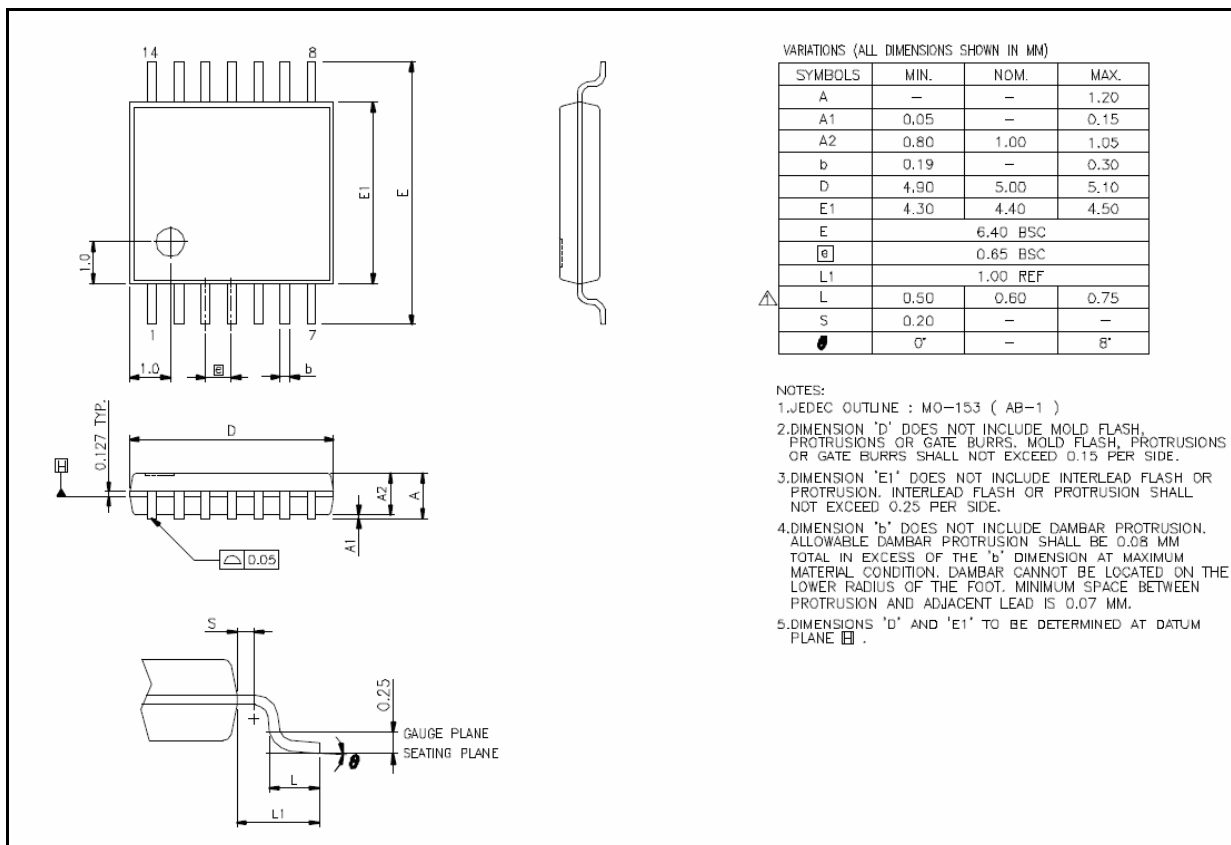
$$RES (\Omega) = [ Vled(V) - Vf(V) - Vce(V) ] / ILED(A)$$



## © AUR6502 Package Specification – SOP14 Outline Drawing



## © AUR6502 Package Specification – TSSOP14 Outline Drawing



## © AUR6502 Package Specification – PDIP14 Outline Drawing

