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AUR6353
3-CHANNEL LED DRIVER with PWM CONTROLLER

Features

- Driver output: Maximum of 100mA per channel with individual external resistor setting
- Maximum driver port voltage of **24**V at OFF state
- Serial-in clock frequency to 25 MHz
- Built-in output buffers for cascading clock, data and strobe
- PWM luminance control capability (refresh rate of 400+ Hz) with an internal oscillator (~ 7 MHz)
- Selectable control modes of PWM output:
  - 8-bits luminance data and 5-bits individual color correction (13 bits mode)
  - 8-bits luminance data and 6-bits global brightness data (14 bits mode)
  - 8-bits luminance data with PWM current output
- Over temperature protection
- Under Voltage Lock-out
- PWM output polarity inversion function
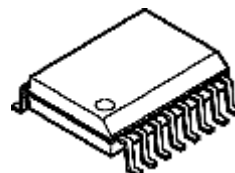- Power supply voltage: **6V ~ 28V**

Description

AUR6353 is a 3-channel (R, G, B) current-regulated LED driver with a high-resolution Pulse Width Modulation (PWM) luminance controller. The chip enables serial data-in and data-out interface with built-in shift registers, internal data latches and storage registers. It is designed ideally for full-color LED decorative or general lighting, signs and display applications.

The output current levels of the low dropout-voltage drivers are established by the built-in BandGap reference voltage with external resistors. One external resistor is used for each channel. Built-in internal oscillator generates a high frequency clocking signal and modulation logic to provide PWM light luminance control with three selectable operation modes. Data, clock and strobe output buffers can be used for cascading with next AUR6353. The PWM output polarity inversion function is designed for controlling other LED drivers especially in high power LED applications.
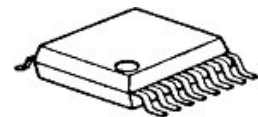
Applications

- LED Decorative Lighting
- LED General Lighting
- PWM Generator and Controller
- Flexible Indoor/Outdoor Video or Sign Displays
- LCD Display Backlighting
- Torch/Warning Signs
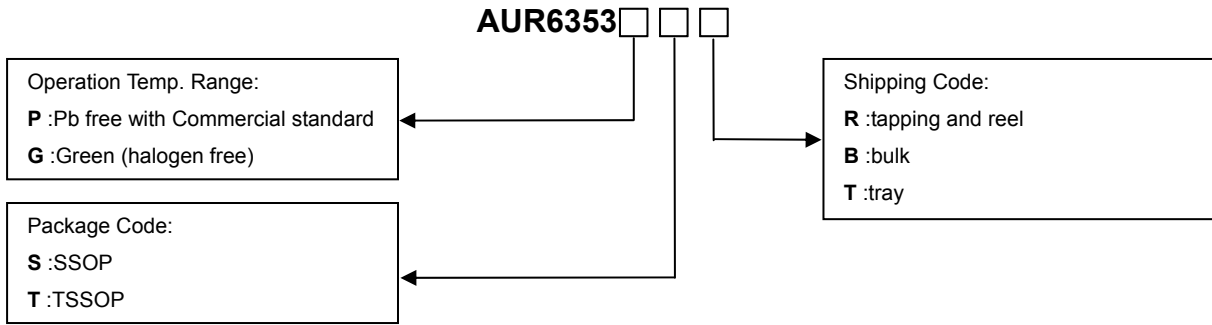- Automotive or Instrument Panel Lighting
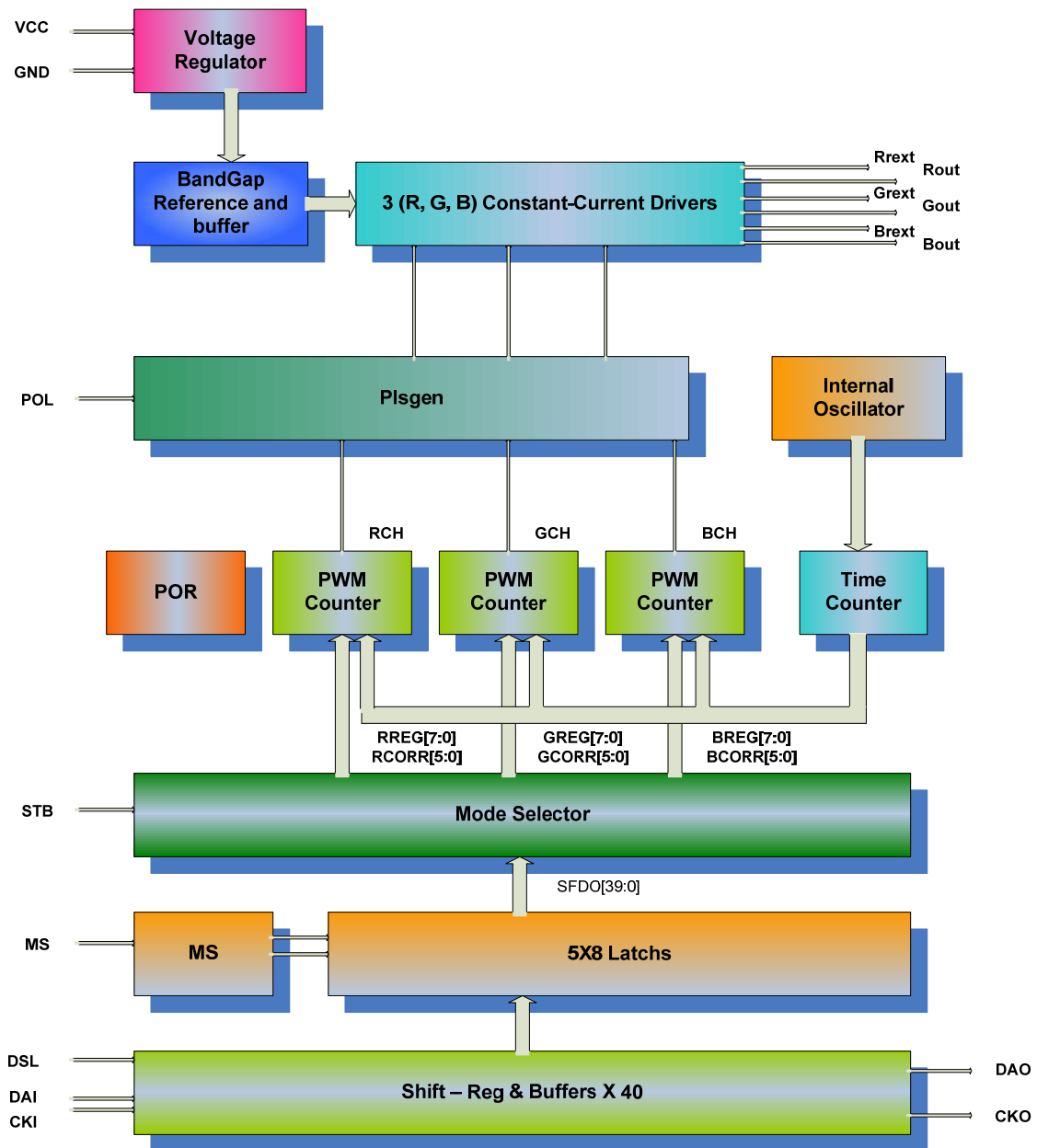
Package Information

SSOP16   TSSOP16

Ordering Information

AUR6353☐ ☐ ☐

Operation Temp. Range:
P :Pb free with Commercial standard
G :Green (halogen free)

Package Code:
S :SSOP
T :TSSOP

Shipping Code:
R :tapping and reel
B :bulk
T :tray

Block Diagram

Typical Application

· POL and SDO are 'Floating'.

Pin Description

```
         ┌──────┐
DAO  ──│1    16│── VCC
CKO  ──│2    15│── DAI
STBO ──│3    14│── CKI
POL  ──│4    13│── /STB
ROUT ──│5    12│── DSL
GOUT ──│6    11│── RREX
BOUT ──│7    10│── GREX
GND  ──│8     9│── BREX
         └──────┘
```
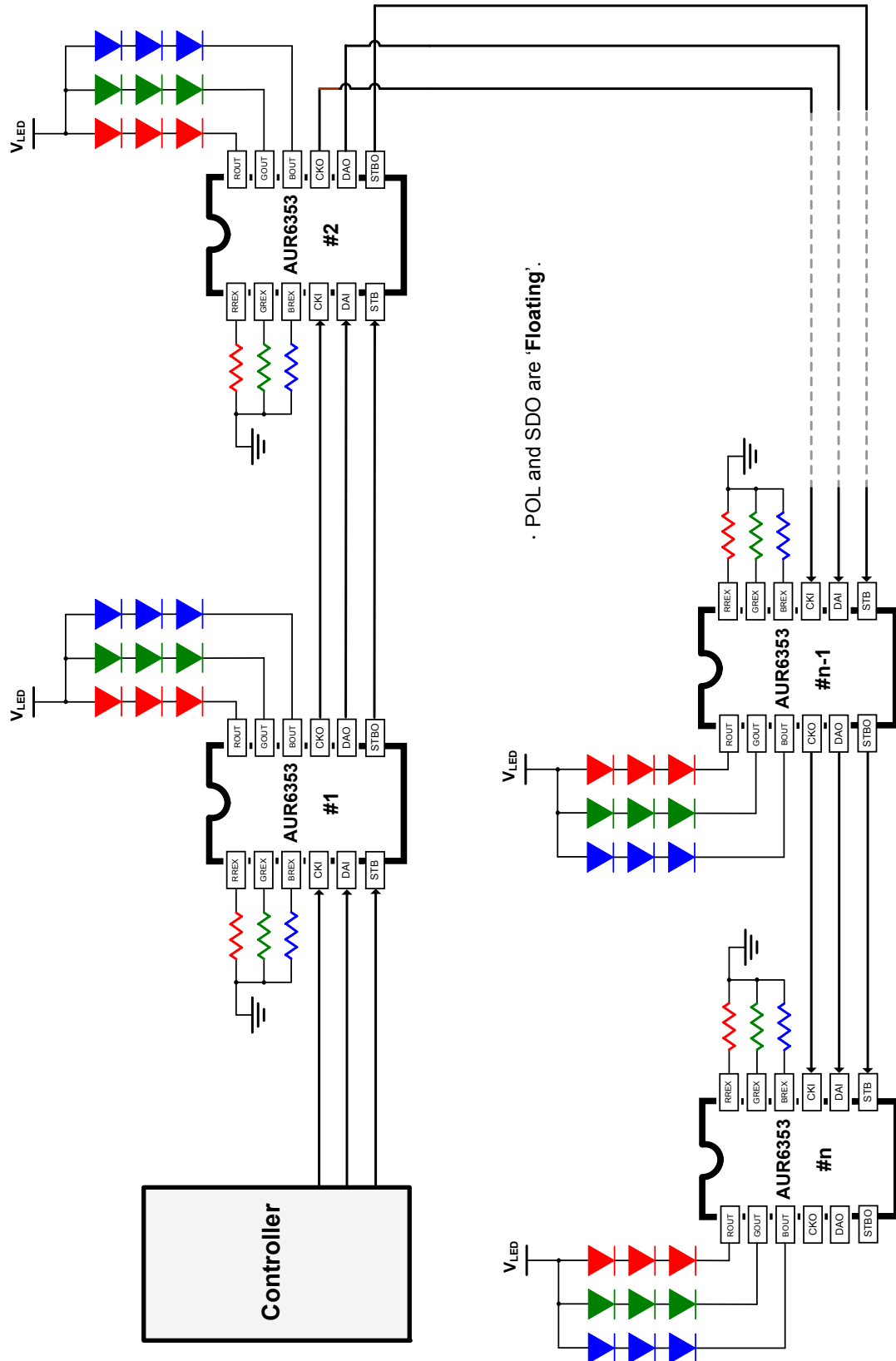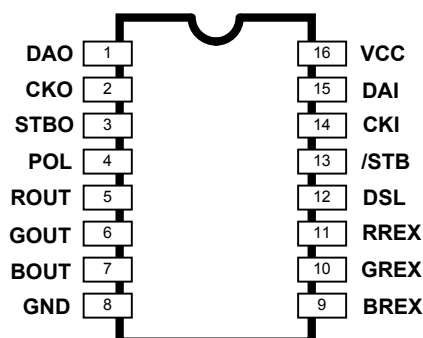
PIN No.	PIN NAME	Pin Type	FUNCTION
1	DAO	DO	Serial data output.
2	CKO	DO	Clock output signal.
3	STBO	DO	Strobe output signal.
4	POL	DI	PWM current output polarity for pulse inversion: "**Floating**" for positive polarity, "**L**" for negative polarity.
5~7	R(G、B)OUT	AO	Open-drain driver current sink.
8	GND	GROUND	Ground Pin
9~11	R(G、B)REX	AI	Driver output current setting pins for external resistor connections between (R, G and B)REX and GND
12	DSL	DI	Serial data output selection: "**Floating**": data to be shifted out at the falling edge of CKO, "**L**" : data to be shifted out at the rising edge of CKO.
13	/STB	DI	Data-input strobe pulse, latches data into internal registers when /STB is low (level latch).
14	CKI	DI	Clock input pin for serial data transfer. Data is sampled at the rising edge of CKI
15	DAI	DI	Serial data input
16	VCC	POWER	Power supply voltage input

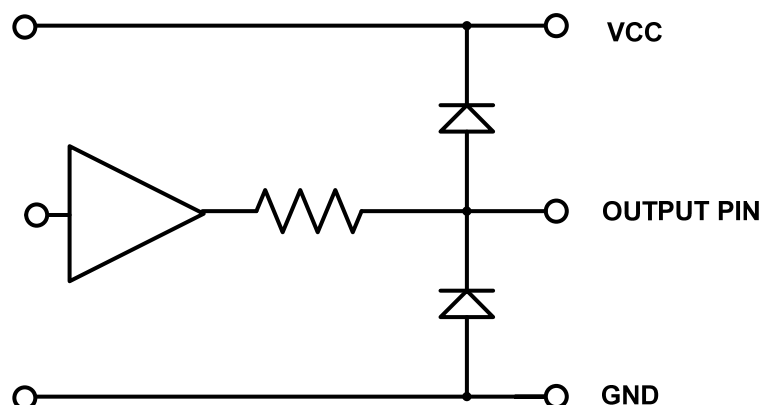# Equivalent Circuit of Inputs and Outputs

1. **CKI, DAI, and /STB Pins**
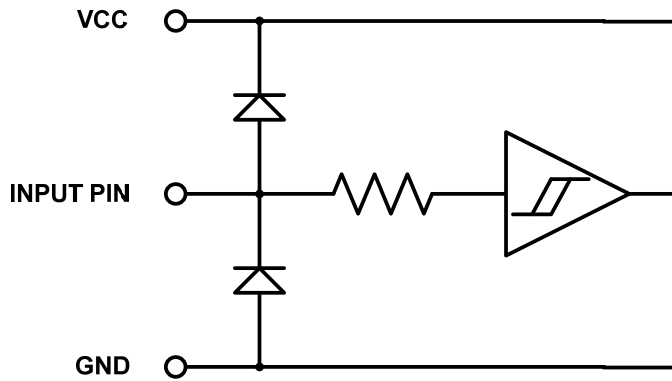
2. **DSL and POL Pins**
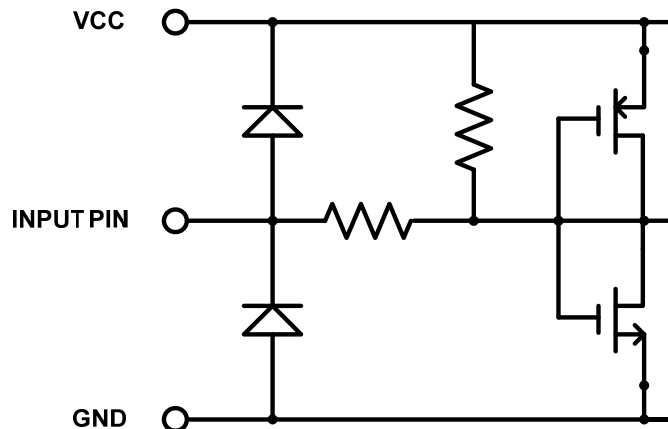
3. **CKO, DAO, and STBO Pins**

Maximum Ratings (Ta = 25°C , Tj(max) = 140°C)

| CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	- 0.3 ~ 30	V
Logic Input Voltage	VIN	- 0.3 ~ **6.0**	V
Driver Output Current	IOUT	120	mA
Driver Output Voltage	VOUT	- 0.3 ~ 24	V
Input Clock Frequency	FCKI	25	MHz
GND Pin Current	IGND	360	mA
Power Dissipation	PD	0.82 (SSOP16 : Ta=25°C) 2.1 (TSSOP16 : Ta=25°C)	W
Thermal Resistance	Rth(j-a)	140.2 (SSOP16) 55 (TSSOP16)	°C/W
Operating Temperature	Top	- 40 ~ 85	°C
Storage Temperature	Tstg	- 55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC		6.0	12	28	V
Driver Output Voltage	VOUT	Driver ON (IOUT = 100mA) (see dropout voltage diagram)		1.0		V
		Driver Off			24	
Output Current	IOUT	(Driver) OUT (R, G, B)	5		100	mA
	IOH	(Logic) SERIAL-OUT			2	
	IOL				- 2	
Logic Input Voltage	VIH	VCC = 6V~28V	4		VCC	V
	VIL		GND		1	
Input Clock Frequency	FCKI	Single Chip Operation	0		25	MHz
STB Pulse Width	twSTB		20			ns
CKI Pulse Width	twCLK		20			
POL Pulse Width	twPOL	VCC = 6V~28V	100			
Set-up Time of DAI	tsetup(D)		25			
Hold Time of DAI	thold(D)		25			
Set-up Time for STB	tsetup(L)		20			
Internal Oscillator Frequency	FOSC	Ta = 25°C VCC = 6V~28V	5.5	7.0		MHz

## Electrical Characteristics(VCC = 12V, Ta = 25°C , Tj(max) = 140°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Input Voltage 'H' Level	VIH	CMOS	4		VCC	V
Logic Input Voltage 'L' Level	VIL	logic level	GND		1	
Driver Output Leakage Current	IOL	VOH = 24V			1.0	µA
Logic Output Voltage (S-OUT)	VOL	IOL = 2mA			0.2	V
	VOH	IOH = -2mA	VCC-0.2			
Driver Output Current Skew (Channel to Channel)	IOL1	VOUT = 1.0V REX = 120Ω			±3	%
Driver Output Current Skew (Chip to Chip)	IOL2				±6	%
Driver Current vs. Output Voltage Regulation	% / VOUT	REX = 120Ω VOUT = 1V~3V		0.1	0.5	% / V
Driver Current vs. Supply Voltage Regulation	% / VCC	REX = 120Ω VCC = 6V~28V			2	
Pull-high Resistor	Rph			200		KΩ
Thermal Shutdown	Tsd		140		160	°C
Supply Current (Analog Portion)	I_{DD_A}	VOUT = 1.0V REXn = 120Ω Driver ON all DI pins are low		4.5		mA

Test Diagram
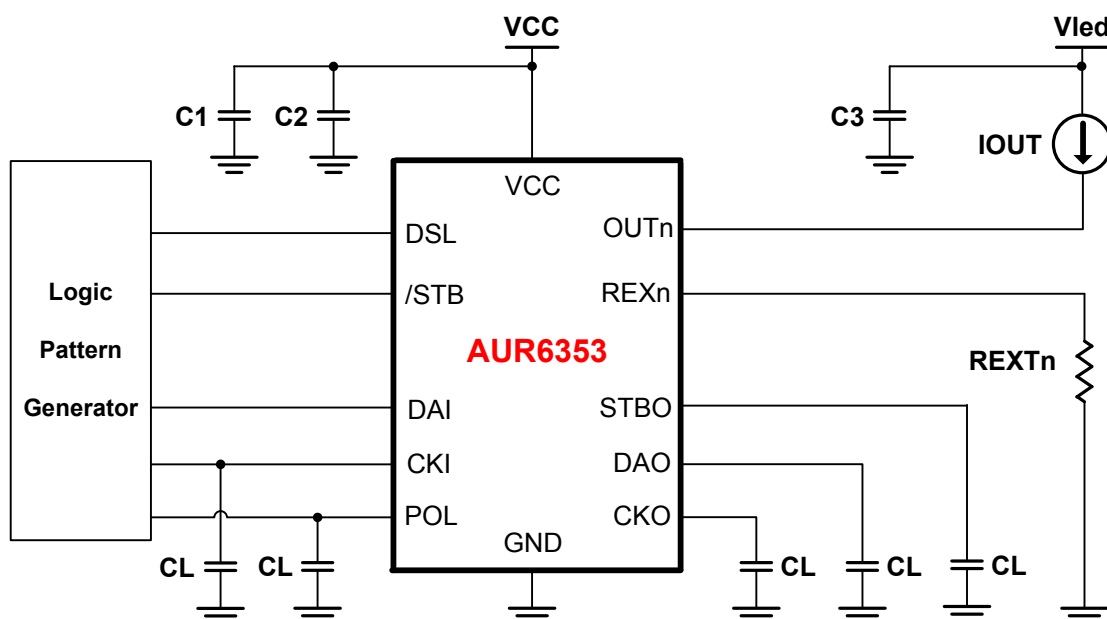
I/O Timing Diagrams:
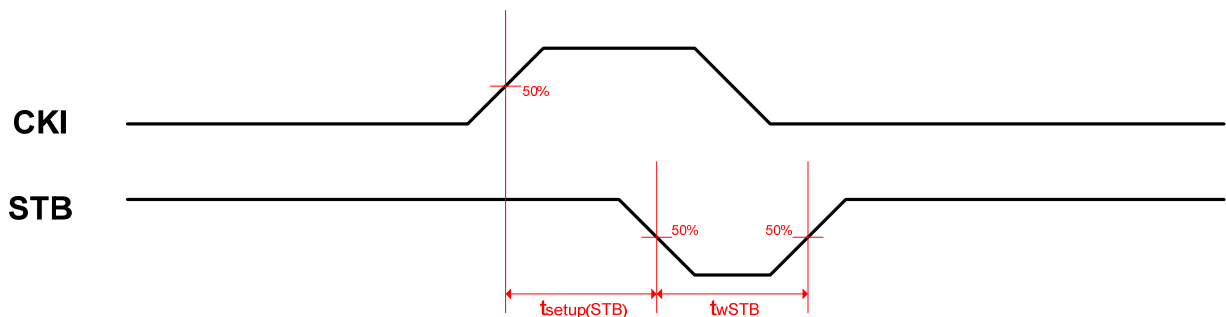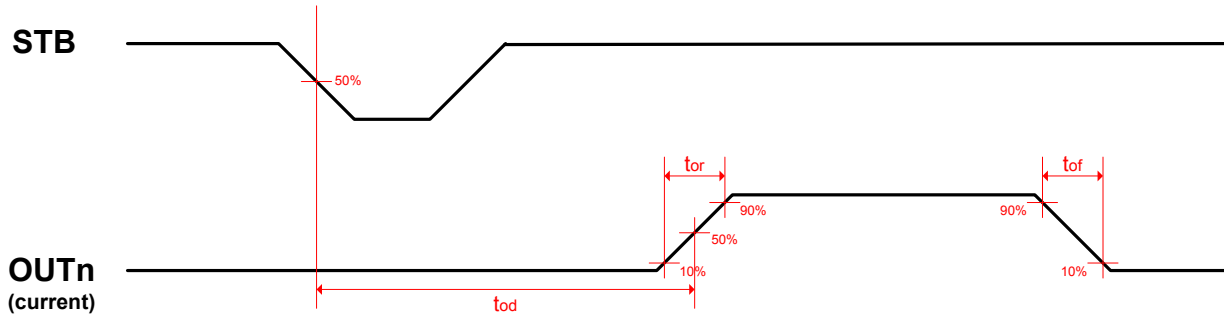
a) Timing of CKI, DAI, CKO and DAO
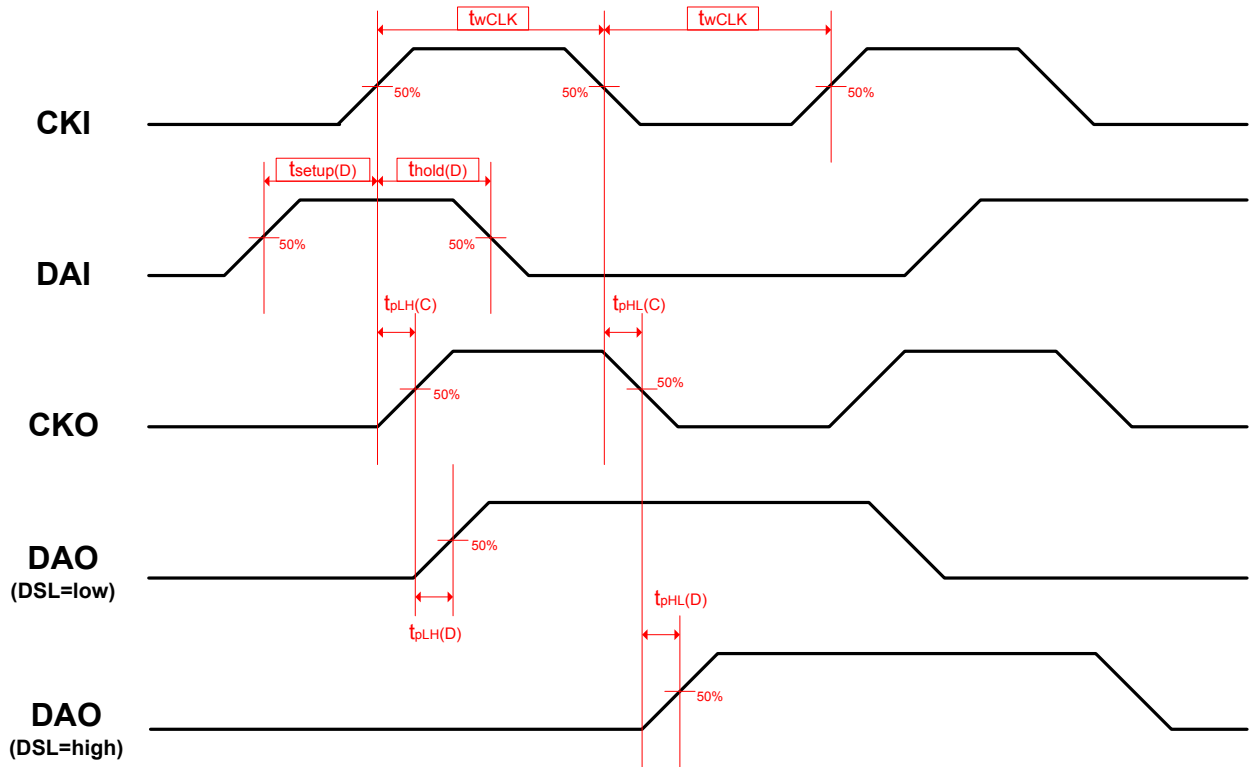
b) Timing of CKI and STB

I/O Timing Diagrams:

c) Timing of STB and OUT

d) Timing of POL and OUT
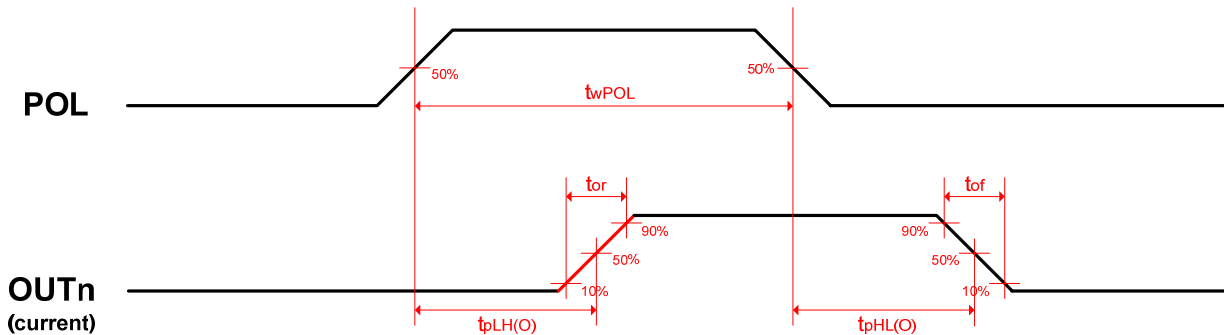
e) Timing of STB and STBO
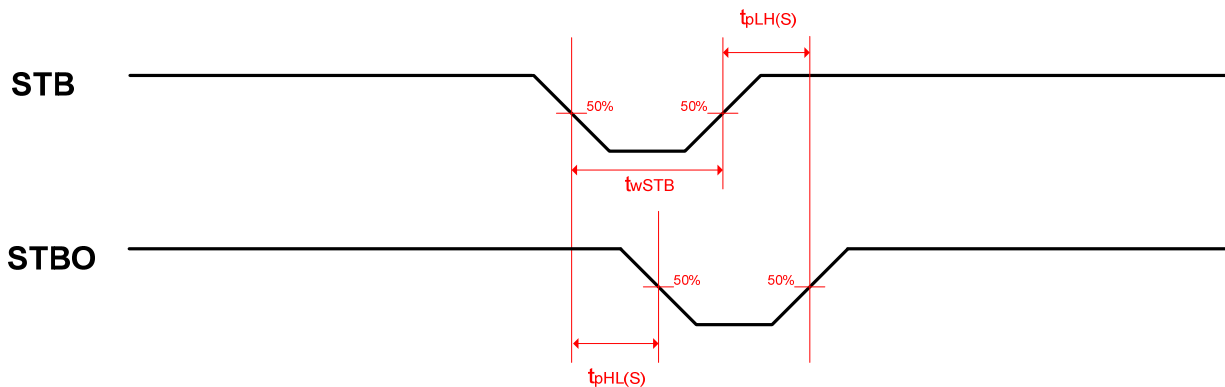
Data Timing Diagrams:
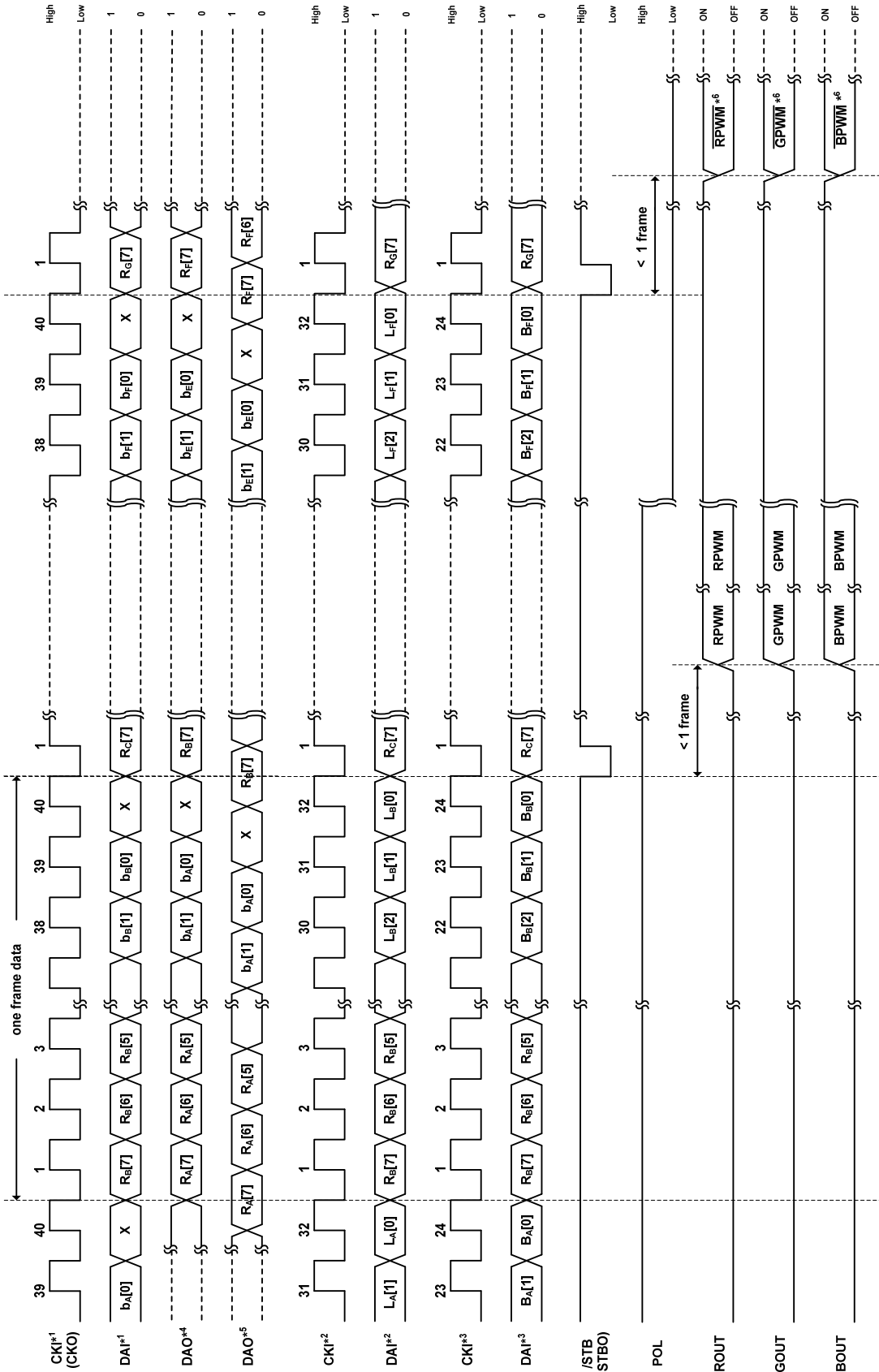
*1 13-bits/5 byte mode.

*2 14-bits/4 byte mode.

*3 8-bits/3 byte mode.

*4 DSL = high

*5 DSL = low

*6 $\overline{PWM}$ means the inverse waveform of PWM.

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Timing Diagrams of Mode Switching:

AUR6353 can provide three control modes of PWM output:

- 8-bit luminance data with 5-bit individual color correction data (13-bit / 5 byte mode)

- 8-bit luminance data with 6-bit global brightness data (14-bit / 4 byte mode)

- 8-bit luminance data only (8 bit / 3 byte mode)

When power turns on, 8 bit / 3 byte mode is the default. Modes are switched by input (DAI, CKI, STB) patterns:
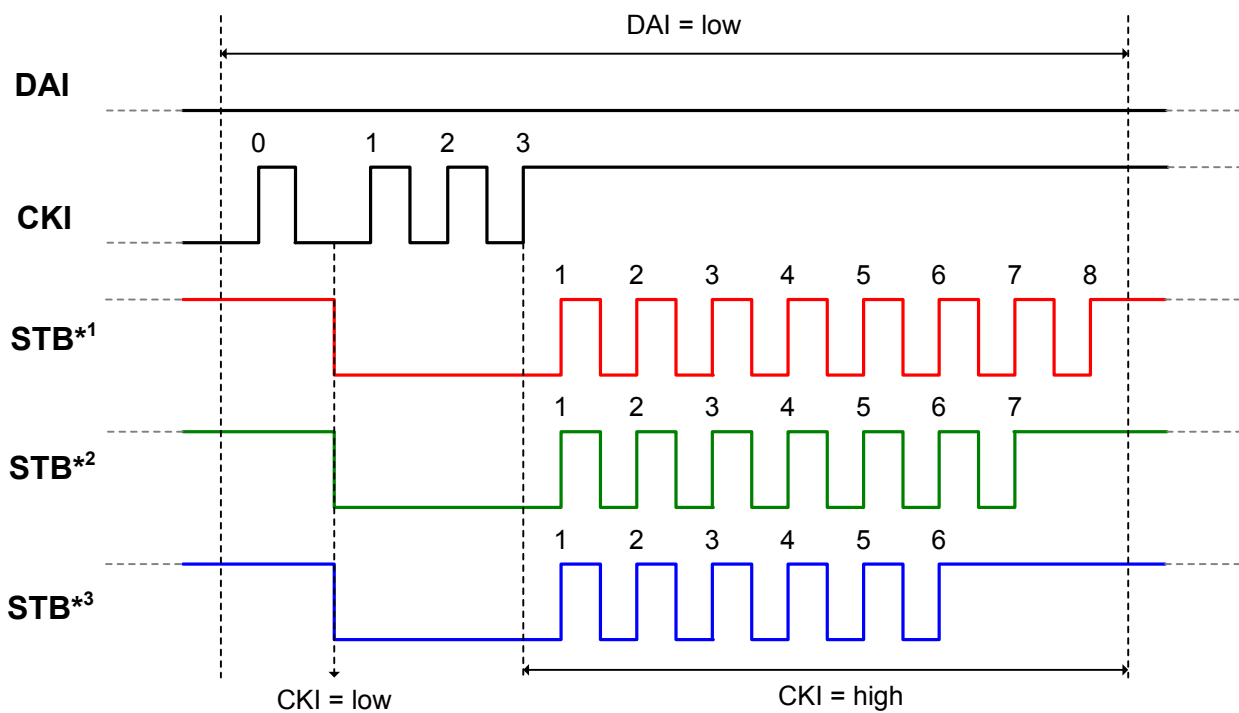
*1 switch to 13-bit / 5 byte mode.

*2 switch to 14-bit / 4 byte mode.

*3 switch to 8-bit / 3 byte mode.

Data Frames and Format:

13-bits / 5byte mode

14-bits / 4byte mode

8-bits / 3byte mode
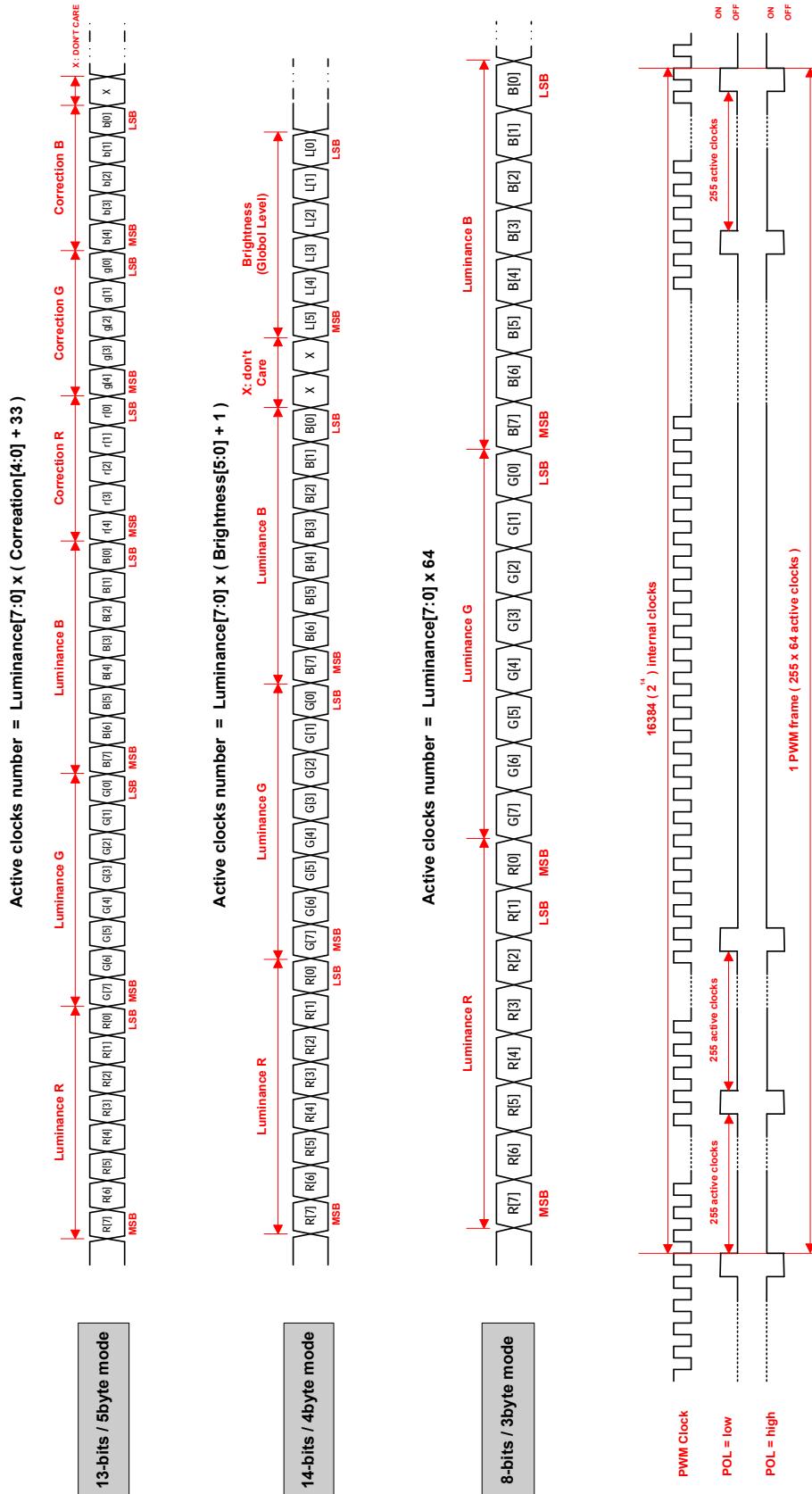
Output Current and Drop-Out Voltage:

The output current level of individual driver is established by an external resistor REX for each channel. The output range of each driver is designed from 5mA to 100mA according to the equation below. It is recommended the voltage at driver output ports should be as low as possible for consideration of power dissipation and constant current operations. If operating driver over working temperature, AUR6350 will go into shutdown mode automatically and recover to normal mode until the junction temperature is lower than 140°C. A characteristic curve of output current levels vs. setting resistor values is displayed in the following diagram.

Iout (A) = 0.6 V / REX Ω
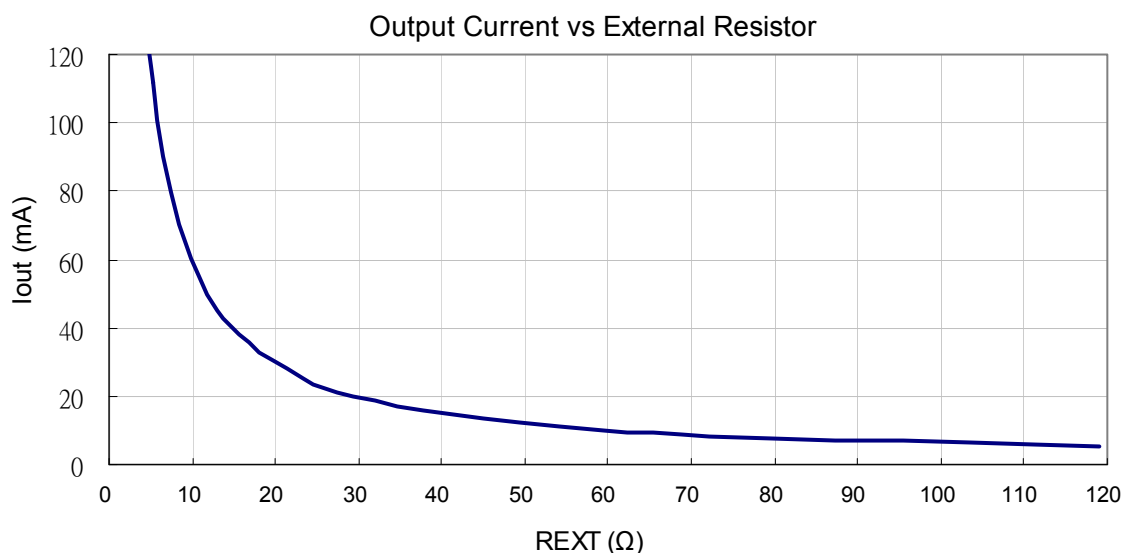
The output current is kept constant for driving multiple LEDs in series with each driver before reaching the dropout voltage limits. LEDs with various forward voltages (V_F) can be used within usable voltage headroom. Typical output current characteristic of an output driver is shown below for illustrating driver dropout voltage vs. output current level.
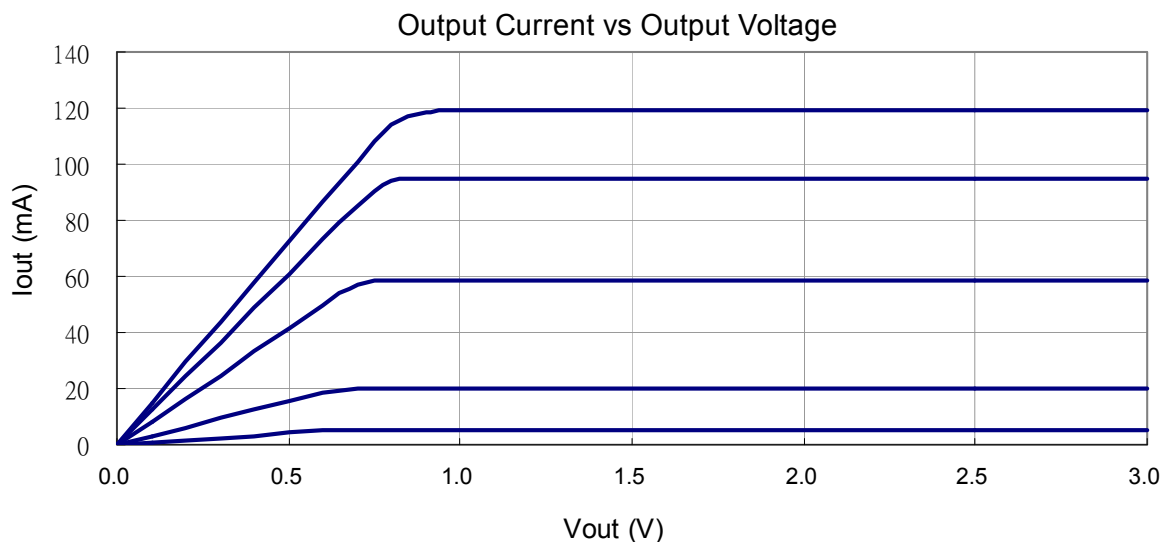
◎ AUR6353 Package Specification – TSSOP16 Outline Drawing

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

⚠ THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
118X11E	2.40	3.00	2.40	3.00

NOTES:
1. JEDEC OUTLINE :
   MO-153 AB/MO-153 ABT(THERMALLY ENHANCED VARIATIONS ONLY)
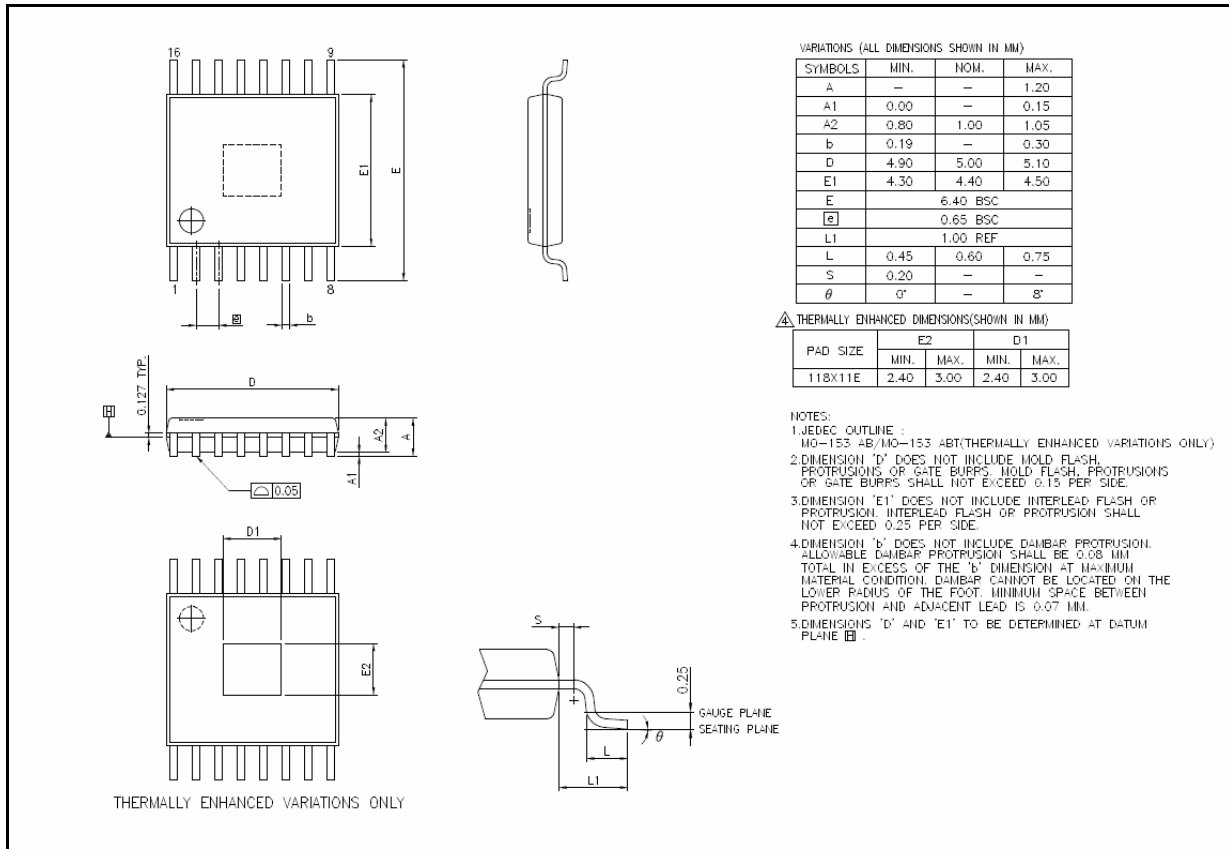2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH,
   PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS
   OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR
   PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL
   NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM
   TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM
   MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE
   LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN
   PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM
   PLANE Ⓗ .

◎ AUR6353 Package Specification – SSOP16 Outline Drawing

SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	–	0.059
b	0.008	0.012
b1	0.008	0.011
c	0.007	0.010
c1	0.007	0.009
D	0.189	0.197
E1	0.150	0.157
E	0.228	0.244
L	0.016	0.050
e	0.025 BASIC	
θ°	0	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MO-137 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH,
   PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS
   AND GATE BURRS SHALL NOT EXCEED .15mm (.006in)
   PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH,
   OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS
   SHALL NOT EXCEED .25mm (.010in) PER SIDE.