LOW-VOLTAGE TOUCH SCREEN CONTROLLER

Features

- Low Power operation for 2.5V TO 5.25V
- Supports Low Voltage Interface for 1.5V to 5.25V Logic Levels
- Pressure Digitization with A 12-bit Resolution
- Built-In BandGap with Internal Voltage Buffer for Providing a 2.5V Voltage Reference
- Temperature Measurement and Digitization
- 2 Digitization Inputs Provide Direct Measurement of Battery Voltage
- Internal Power-On-Reset (POR)
- Support 3 Modes of I^2C Interface: Standard, Fast and High-speed
- Available TSSOP-16 Package

Applications

- Mobile Phones
- Personal Digital Assistants
- Smart Hand-held or Gaming Devices
- Touch Screen monitors
- Point-of-sales Terminals
- Digital Frame Devices
- GPS and Pagers

Order Information

AUR3843**P**□□ AUR3843**G**□□	P: Pb free with commercial standard G: Green (halogen free with commercial standard)
AUR3843□**T**□	T: TSSOP16 Package
AUR3843□□**R** AUR3843□□**B** AUR3843□□**T**	R: tapping and reel B: bulk T: tray

Description

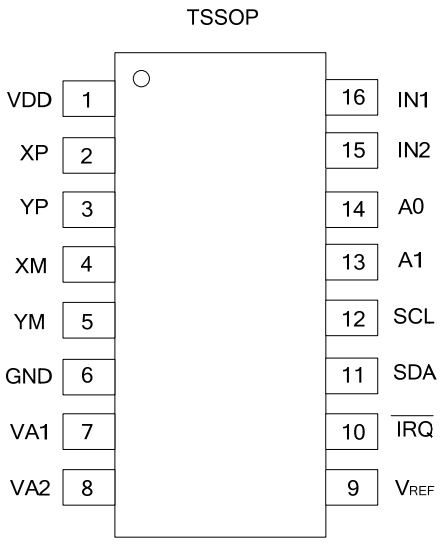
The AUR3843 supports 4-wire touch screen control for low power operational devices. It includes a 12-bit successive approximation analog-to-digital (ADC) converter with an I^2C interface and low power switches for flexible measurement of touch screen pressure.

An accurate Bandgap reference voltage is built-in and associated with a temperature detection circuit for an on-chip digital temperature measurement. Two auxiliary analog inputs are also provided for digitization with the ADC. Other two battery measurement inputs are offered for smart power monitoring and management needs.

An on-chip 2.5V reference voltage buffer circuit is available to either internal or external usages. AUR3843's internal reference source operates down to 2.5V supply voltage with optimized power consumption, while monitoring the battery voltage from 0.5V to 6V. It is an ideal choice for battery operated systems for power saving and green operations. The AUR3843 is available in TSSOP-16 package and is specified over the temperature range of –40°C to +85°C.

Pin Configuration

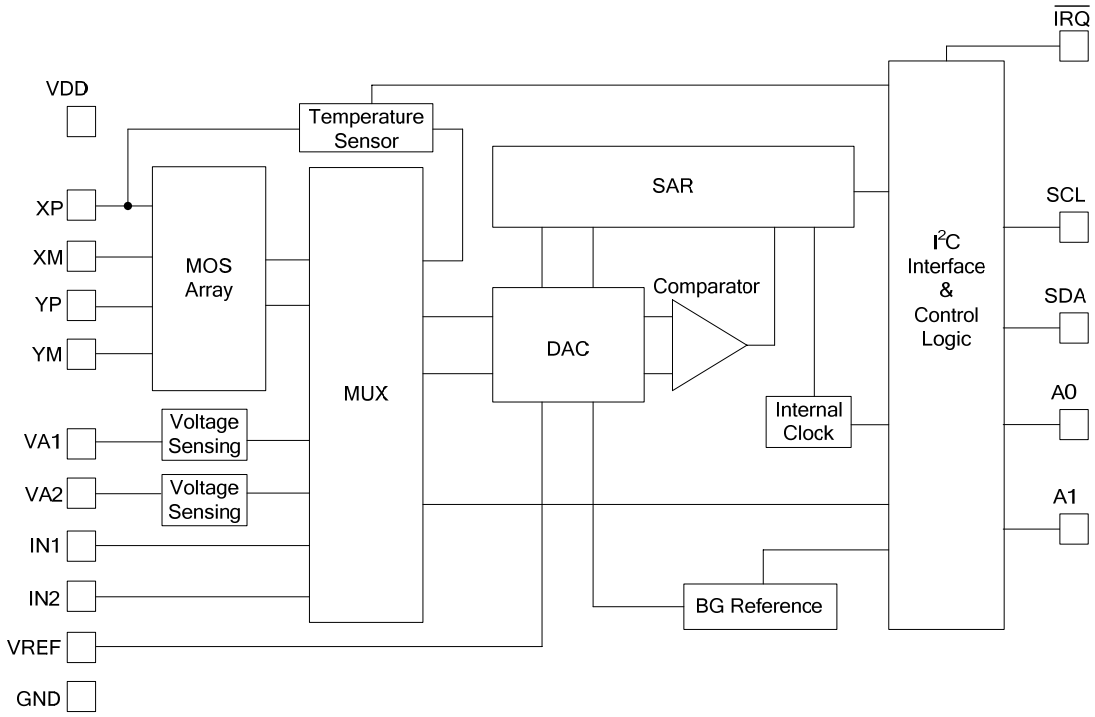
TSSOP



Pin Description

TSSOP PIN	PIN NAME	PIN TYPE	FUNCTION
1	VDD	POWER	Power Supply
2	XP	AI	XP Contact Pin
3	YP	AI	YP Contact Pin
4	XM	AI	XM Contact Pin
5	YM	AI	YM Contact Pin
6	GND	GROUND	Ground
7	VA1	AI	Battery Monitor Input 1
8	VA2	AI	Battery Monitor Input 2
9	VREF	AI/AO	Voltage Reference Input/Output
10	$\overline{IRQ}$	DO	Interrupt Request
11	SDA	DI/DO	Serial Data
12	SCL	DI/DO	Serial Clock
13	A1	DI	I^2C Bus Address Input A1
14	A0	DI	I^2C Bus Address Input A0
15	IN2	AI	Auxiliary A/D Converter Input
16	IN1	AI	Auxiliary A/D Converter Input

Block Diagram



Absolute Maximum Rating

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	- 0.3 ~ + 6.0	V
Analog Input Voltage (Pins 7, 8)		- 0.3 ~ + 6.0	V
Analog Input Voltage (Other pins)		- 0.3 ~ VDD + 0.3	V
Logic Input Voltage		- 0.3 ~ VDD + 0.3	V
Power Dissipation	PD	250	mW
Maximum Junction Temperature	Tj	150	°C
Operating Temperature	Top	- 40 ~ 85	°C
Storage Temperature	Tstg	- 65 ~ 150	°C

Electrical Characteristics

At T_A=–40°C to +85°C, VDD=+2.7V, VREF=2.5V external voltage, I^2C bus frequency=3.4MHz, 12-bit mode and digital inputs = VDD or GND, unless otherwise noted.

CHARACTERISTIC	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC Accuracy					
Resolution			12		Bits
No Missing Codes	Standard/Fast modes	11			Bits
	High-speed mode	10			Bits
Integral Linearity Error	Standard/Fast modes			±2	LSB
	High-speed mode			±4	LSB
Offset Error				±6	LSB
Gain Error	External VREF			±4	LSB
Noise	Including Internal VREF		70		μVrms
Power-Supply Rejection			70		dB
MOS Array					
On-Resistance					
YP, XP			5.5		Ω
YM, XM			7.3		Ω
Drive Current	Duration 100ms			50	mA
Analog Input					
Full-Scale Input Span	Positive-Negative Input	0		VREF	V
Absolute Input Range	Positive Input	-0.2		+VDD+0.2	V
Capacitance			25		pF
Leakage Current			0.1		uA
SAMPLING DYNAMICS					
Throughput Rate			50		ksps
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
REFERENCE OUTPUT					
Internal Reference Voltage		2.45	2.50	2.55	V
Internal Reference Drift			25		ppm/°C
Output Impedance	Internal Reference On		300		Ω

	Internal Reference Off		1		GΩ
Quiescent Current	PD1=1, PD0=0, SDA, SCL High		750		µA
REFERENCE INPUT					
Range		2.0		+VDD	V
Input Impedance	PD1 = PD0 = 0		1		GΩ
BATTERY MONITOR					
Input Voltage Range		0.5		6.0	V
Input Impedance	Sampling Battery		10		KΩ
	Battery Monitor Off		1		GΩ
Accuracy	External V_{REF}=2.5V	-2		+2	%
	Internal Reference	-3		+3	%
TEMPERATURE MEASUREMENT					
Temperature Range		-40		+85	°C
Resolution	Differential Method		1.6		°C
	TEMP0		0.3		°C
Accuracy	Differential Method		±2		°C
	TEMP0		±3		°C
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
V_{IH}	$\lvert I_{IH} \rvert \leqq +5\mu A$	VDD • 0.7		VDD + 0.3	V
V_{IL}	$\lvert I_{IL} \rvert \leqq +5\mu A$	–0.3		VDD •0.3	V
V_{OH}	$I_{OH} = -250\mu A$	VDD • 0.8			V
V_{OL}	$I_{OL} = 250\mu A$			0.4	V
$\overline{IRQ}$ V_{OL}	30kW Pull-Up		Straight		
Data Format			Binary		
Input Capacitance	SDA, SCL Lines			10	pF
POWER-SUPPLY					
VDD	Specified Performance	2.7		3.6	V
	Operating Range	2.5		5.25	V
Quiescent Current	Internal Reference Off,				
	PD1 = PD0 = 0				
	High-speed mode: SCL = 3.4MHz		254	650	uA
	Fast mode: SCL = 400kHz		95		uA
	Standard mode: SCL = 100kHz		63		uA
	Internal Reference On, PD0 = 0		1005		uA
Power-down Current when Part is	Internal Reference Off,				
not Addressed	PD1 = PD0 = 0				
	High-speed mode: SCL = 3.4MHz		90		uA
	Fast mode: SCL = 400kHz		21		uA
	Standard mode: SCL = 100kHz		4		uA
	PD1 = PD0 = 0, SDA = SCL = VDD			3	uA
Power Dissipation	VDD = +2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		-40		+85	°C

Circuit Information

1. General

The AUR3843 offers Successive Approximation Register (SAR) ADC circuit with I^2C interface. Figure 1 shows a connection diagram for AUR3843 in a touch screen control application.

The AUR3843 can be operated from a 2.7V to 5.25V power supply. The throughput rate could be 125kSPS with 2MHz clock. AUR3843 features an internal reference and uses an internal clock. The internal reference can be driven with an external low impedance source between 2V and VDD. The value of the reference voltage sets the input range of the converter.

The analog input to the converter is provided via a multiplexer that can be connected to the touch screen position sensing signals, battery voltage, auxiliary input signal, or the chip temperature sensing voltage. For the reasons of power saving and minimizing ADC conversion errors due to finite on-resistance of the built-in switches, differential configurations could be applied to both the conversion input signals and reference voltage sources for optimized performance.

2. ADC Transfer Function

The digital output coding of the AUR3843 is straight binary. The ideal transfer function is shown in Figure 2.

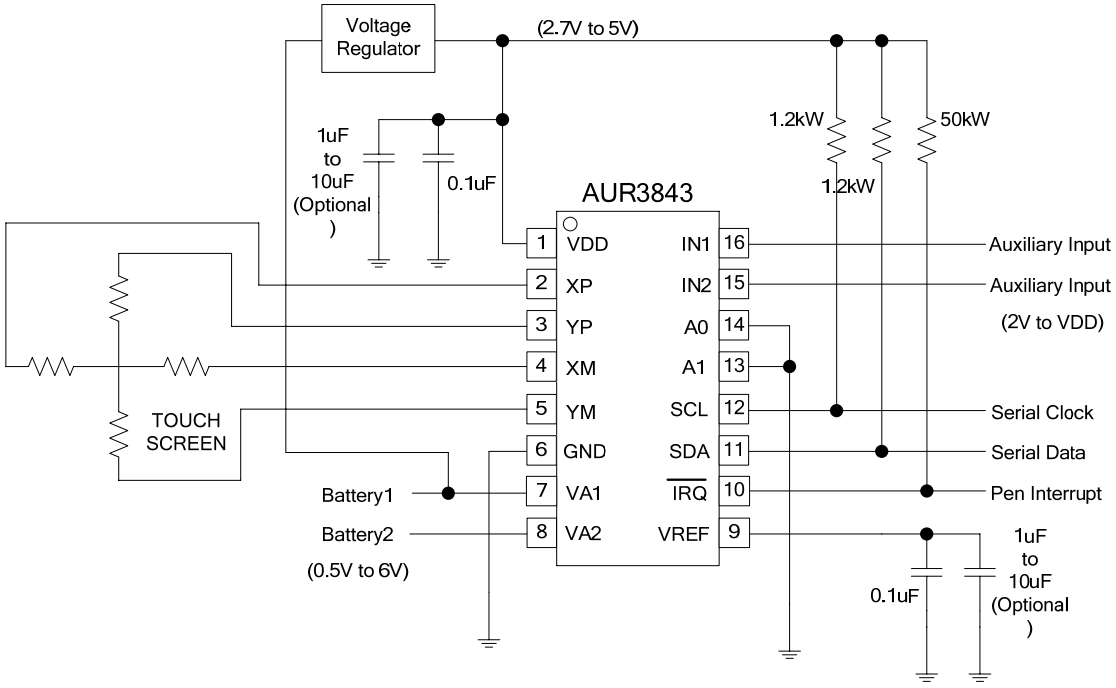


Figure 1. Typical Application Circuit

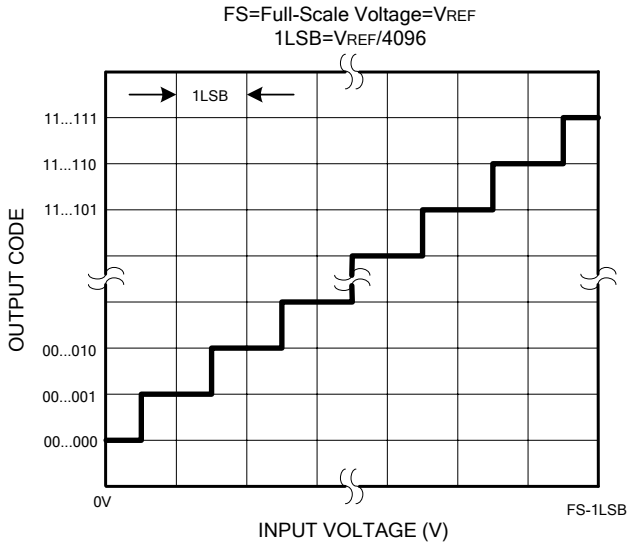


Figure 2. Ideal Input Voltages and Output Codes

3. Analog Input to ADC

The input of ADC is selected by a multiplexer as shown in Figure 3 with an address setting according to Table 1. The control bits are provided serially via the I^2C interface.

The voltage between the +IN and –IN is captured on the internal capacitor array during the hold mode. When the converter enters the sample mode, the source must charge the internal sampling capacitor. An ADC conversion starts after the capacitor is fully charged from the input circuit.

4. ADC Conversion

The differential voltage of +REF and -REF defines the full swing voltage of ADC input with register settings as shown in Table 1. The conversion range of AUR3843 covers 2V to VDD. The ADC conversions can be made in differential mode or single-ended mode according the register setting. In single-ended mode, the +REF is connected to VREF and –REF is connected to GND. Usually the VREF was connected to VDD to obtain the maximum full swing voltage for ADC conversion range. The switch array can be turned off beside the acquisition time to save the power.

When the switches are on, the touch screen measurement operations can be performed. Because of the finite on-resistance of the switches, the voltage on XP/YP and XM/YM may not be same as set to be VDD and GND, so that true full-scale and zero-scale conversion is not possible. This situation can be improved in a differential mode as stated previously.

In the differential mode, the +REF and -REF of ADC was obtained by the sampling voltages of XP (or YP) and XM (or YM), respectively. This makes the ADC conversion ratiometric. The result of the conversion is always a percentage of the external resistance, independent of the on-resistance of the internal switches.

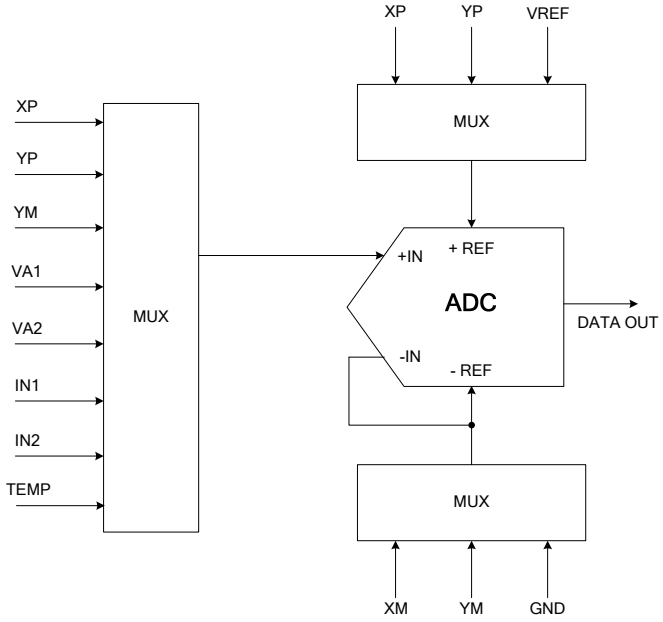


Figure 3. Analog Input Circuit

C3	C2	C1	C0	Function	ADC Input	X Switches	Y Switches	Mode	+ REF	- REF
0	0	0	0	Measure TEMP0	TEMP0	OFF	OFF	SER	VREF	GND
0	0	0	1	Measure VA1	VA1	OFF	OFF	SER	VREF	GND
0	0	1	0	Measure IN1	IN1	OFF	OFF	SER	VREF	GND
0	0	1	1	Not Use						
0	1	0	0	Measure TEMP1	TEMP1	OFF	OFF	SER	VREF	GND
0	1	0	1	Measure VA2	VA2	OFF	OFF	SER	VREF	GND
0	1	1	0	Measure IN2	IN2	OFF	OFF	SER	VREF	GND
0	1	1	1	Not Use						
1	0	0	0	XM Switches ON		ON	OFF	DFR		
1	0	0	1	YM Switches ON		OFF	ON	DFR		
1	0	1	0	XM, YP Switches ON		XM ON	YP ON	DFR		
1	0	1	1	Not Use						
1	1	0	0	Measure X Position	YP	ON	OFF	DFR	XP	XM
1	1	0	1	Measure Y Position	XP	OFF	ON	DFR	YP	YM
1	1	1	0	Measure Z_1 Position	XP	XM ON	YP ON	DFR	YP	XM
1	1	1	1	Measure Z_2 Position	YM	XM ON	YP ON	DFR	YP	XM

Table 1. Input Setup

5. Digital Operation and Interface

The AUR3843 is designed with an I^2C data interface which performs standard mode (100KHz clock rate), fast mode (400KHz clock rate) and high-speed mode (3.4MHz clock rate) operations. SDA is the serial data signal line and SCL is the clock signal line. Both SDA and SCL signal lines are open-drain I/O type. The chip operates as a slave on an I^2C bus that can be controlled by a master in the bus configuration as either a transmitter or receiver. Figure 4 and 6 illustrate a typical data transfer sequence on the I^2C bus.

The bus operating conditions can be defined as:

(1) START (S) Condition: The SDA changes from High to Low when SCL is High.

(2) STOP (P) Condition: SDA state changes from Low to High when SCL is high.

The I^2C bus is set to be busy after the START condition and considered to be free again a certain time after the STOP condition. A High or Low bit information on SDA data line is valid during the high level of the SCL clock line. The level of SDA must be maintained stable during the entire time that the clock remains High to avoid misinterpretation as a START or STOP condition.

All data blocks are composed of 8 bits. The initial block has 7 address bits followed by a direction bit (Read or Write) with following blocks of 8 data bits. Acknowledge bits are squeezed in between each block. Each data byte is transmitted MSB first including the address byte. The acknowledge bit (generated by the receiving device) indicates to the transmitter that the data transfer was ok. Therefore a data communication is established as 8-bit bytes are exchanged, each one being acknowledged using a 9th data bit generated by the receiving side until the data transfer is complete.

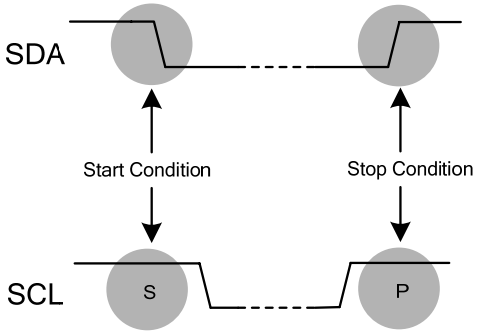


Figure 4. Start and Stop Conditions

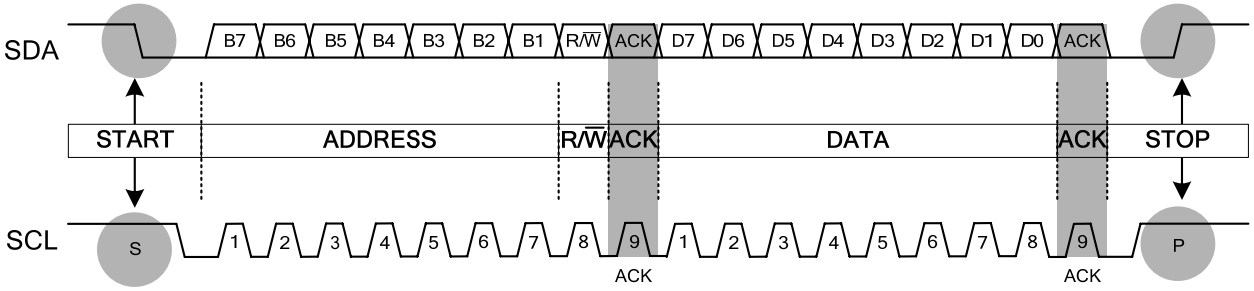


Figure 5. Bus Interface with SCL and SDA for Data Transferring

Each device used on the I^2C bus must have a unique address. A basic Master to slave read or write sequence for I^2C follows that: master device sends the sequence S ADDR W and then waits for an acknowledge bit (A) from the slave which the slave will only generate if its internal set address matches the value sent by the master (see Figure 6). If this

happens then the master sends DATA and waits for acknowledge (A) from the slave. The master completes the byte transfer by generating a stop bit (P) (or repeated start).

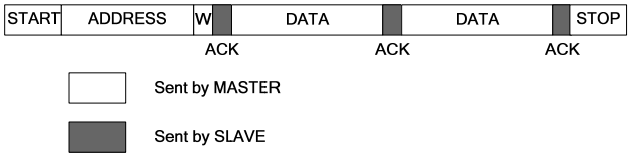


Figure 6. Data Transfer from Master to Slave

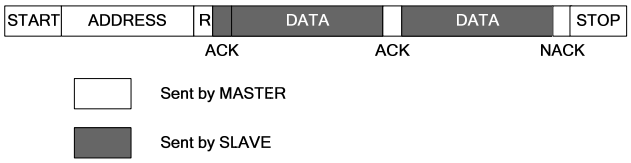


Figure 7. Data Transfer from Slave to Master

A similar process happens when a master reads from the slave, but instead of W, R is sent. After the data is transmitted from the slave to the master the master sends back the acknowledge (A) bit. In the case that master does not want any more data from the slave then it must send out a not-acknowledge which shows to the slave that it should release the bus. This allows the master to send the STOP or repeated START signal.

6. Address and Control Bytes

The first byte transmitted by a master to save device is the address byte. The bits in address byte of AUR3843 are shown in Table 2 and are defined as follows:

(1) First 5 bits: preset to 10010 in factory.

(2) A1, A0: device select bits.

(3) R/$\overline{W}$ bit: select read or write operation (Read operation is performed when R/$\overline{W}$ sets to HIGH).

By sending HIGH or LOW to input pins of A1 and A0, the AUR3843 can be given an address in the bus configuration for up to 4 devices to be connected to the same bus, and master device can control them by setting different address.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	0	A1	A0	R/$\overline{W}$

Table 2. Address Byte

The control byte can determine operating modes of AUR3843. The control bits are shown in Table 3.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C3	C2	C1	C0	PC1	PC0	MC	X

Table 3. Control Byte

(1) C3 to C0: control bits to select operating functions of AUR3843 as defined in Table 1 for the input setup.

(2) PC1, PC0: power down/enable and internal reference control bits. AUR3843 can operate with the lowest power as a control byte to be sent right after power-up. Table 4 shows the control byte configuration.

(3) MC: ADC mode control bit. By setting it to HIGH, 8-bit mode is selected. By setting it to LOW, 12-bit mode is selected.

(4) X: don't care.

PC1	PC0	$\overline{IRQ}$	DESCRIPTION
0	0	Enabled	Power Down between Conversions
0	1	Disabled	Reference is off and ADC is on
1	0	Enabled	Reference is on and ADC is off
1	1	Disabled	Reference is on and ADC is on

Table 4. Control Byte of Power down/Enable and Reference selection

7. Digital Interface Timing

Figure 8 show the detailed timing diagram of AUR3843. Table 5 is the corresponding specification.

8. Interrupt Request

The pen interrupt function is enabled by register PC0 as shown in Table 4. If the function is enabled, the $\overline{IRQ}$ pin goes low when the touch screen is touched. If the screen is not touched, the $\overline{IRQ}$ pin stays high.

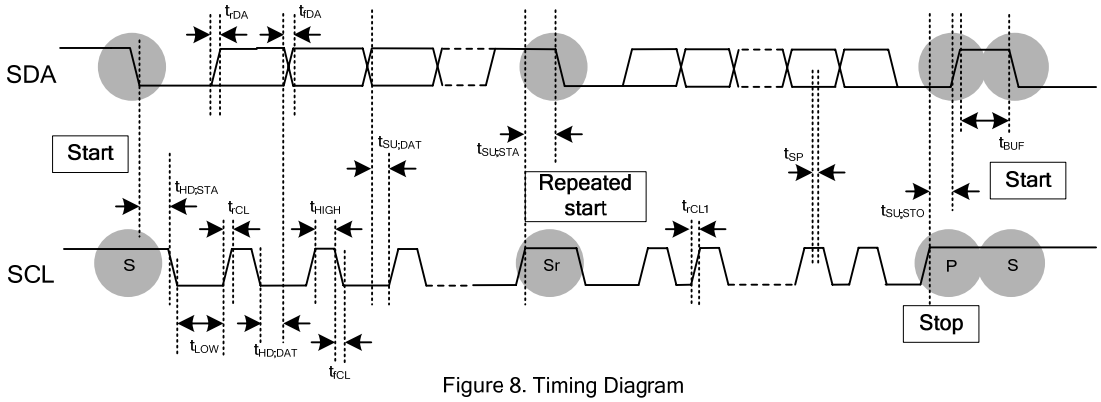


Figure 8. Timing Diagram

TIMING CHARACTERISTICS

At T_A=–40°C to +85°C, VDD=+2.7V, unless otherwise noted. All values referred to V_{IHMIN} and V_{ILMAX} levels.

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	0	100	kHz
		Fast mode	0	400	kHz
		High-speed mode, C_b= 100pF max	0	3.4	MHz
		High-speed mode, C_b= 400pF max	0	1.7	MHz
Hold Time (Repeated) Start Condition	$t_{HD; STA}$	Standard mode	4.0		µs
		Fast mode	600		ns
		High-speed mode	160		ns
Data Hold Time	$t_{HD; DAT}$	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		High-speed mode, C_b= 100pF max	0	70	ns
		High-speed mode, C_b= 400pF max	0	150	ns
Data Setup Time	$t_{SU; DAT}$	Standard mode	250		ns
		Fast mode	100		ns
		High-speed mode	10		ns
Setup Time for a Repeated Start Condition	$t_{SU; STA}$	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		ns
Rise Time of SDA Signal	t_{rDA}	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_b	300	ns
		High-speed mode, C_b= 100pF max	10	80	ns
		High-speed mode, C_b= 400pF max	20	160	ns
Fall Time of SDA Singal	t_{fDA}	Standard mode		300	ns
		Fast mode	20 + 0.1 C_b	300	ns
		High-speed mode, C_b= 100pF max	10	80	ns
		High-speed mode, C_b= 400pF max	20	160	ns
Rise Time of SCL Signal	t_{rCL}	Standard mode		1000	ns

		Fast mode	20 + 0.1 C_b	300	ns
		High-speed mode, C_b= 100pF max	10	40	ns
		High-speed mode, C_b= 400pF max	20	80	ns
Rise Time of SCL Signal after a Repeated Start Condition and after an Acknowledge Bit	t_{rCL1}	Standard mode		1000	ns
		Fast mode	20 + 0.1 C_b	300	ns
		High-speed mode, C_b= 100pF max	10	80	ns
		High-speed mode, C_b= 400pF max	20	160	ns
Fall Time of SCL Signal	t_{fCL}	Standard mode		300	ns
		Fast mode	20 + 0.1 C_b	300	ns
		High-speed mode, C_b= 100pF max	10	40	ns
		High-speed mode, C_b= 400pF max	20	80	ns
HIGH Period of the SCL Clock	t_{HIGH}	Standard mode	4.0		µs
		Fast mode	600		ns
		High-speed mode, C_b= 100pF max	60		ns
		High-speed mode, C_b= 400pF max	120		ns
LOW Period of the SCL Clock	t_{LOW}	Standard mode	4.7		µs
		Fast mode	1.3		µs
		High-speed mode, C_b= 100pF max	160		ns
		High-speed mode, C_b= 400pF max	320		ns
Pulse Width of Spike Suppressed	t_{SP}	Fast mode	0	50	ns
		High-speed mode	0	10	ns
Setup time for Stop Condition	$t_{SU;\ STO}$	Standard mode	4.0		µs
		Fast mode	600		ns
		High-speed mode	160		ns
Bus Free Time Between a Stop and Start Condition	t_{BUF}	Standard mode	4.7		µs
		Fast mode	1.3		µs
Capacitive Load for SDA and SCL Line	C_b	Standard mode		400	pF
		Fast mode		400	pF
		High-speed mode, SCL = 1.7MHz		400	pF
		High-speed mode, SCL = 3.4MHz		100	pF
Noise Margin at High Level for Each Connected Device	V_{nH}	Standard mode Fast mode High-speed mode	0.2VDD		V
Noise Margin at High Level for Each Connected Device	V_{nL}	Standard mode Fast mode High-speed mode	0.1VDD		V

Table 5. Timing Characteristics

9. Temperature Measurement

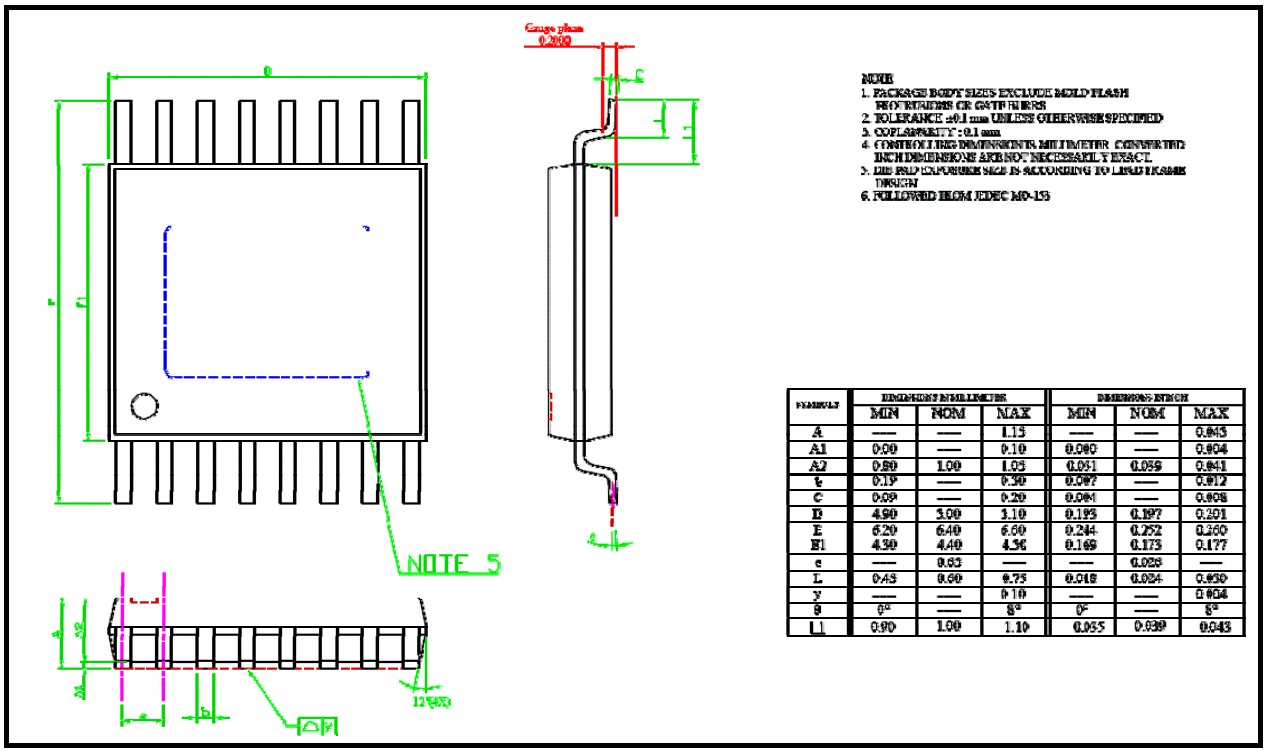
The temperature measurement circuit as implemented relies on the on-chip diode with its forward voltage (V_{BE}) that has a well-defined characteristic versus temperature. The circuit offers two temperature measuring modes. The first mode is the single conversion mode with the diode voltage stored at a known calibration temperature, and then the ambient temperature can be estimated by the subsequent polling of the diode. The second mode operates a two-step measurement. The first step is performed with a fixed bias current into a diode, and the second step is performed with a 91 times larger bias current into the same diode. The voltage difference in the diode is proportional to absolute temperature. The second mode can improve the absolute

temperature measurement over the first mode.

10. Battery Measurement

The AUR3843 is able to monitor the battery voltage from 0.5V to 6V. The input voltage is divided by 4 before entering the ADC circuit. To save the power, the divider is turned on only during the sampling of a voltage on the battery.

Package Information



SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.15	—	—	0.045
A1	0.00	—	0.10	0.000	—	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
C	0.09	—	0.20	0.004	—	0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.50	4.40	4.56	0.169	0.173	0.177
e	—	0.65	—	—	0.026	—
L	0.45	0.60	0.75	0.018	0.024	0.030
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°
L1	0.90	1.00	1.10	0.055	0.039	0.043

Figure 9. AUR3843 TSSOP16 Package Information